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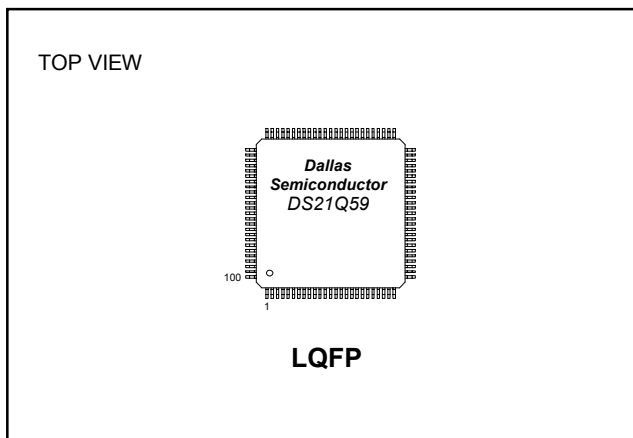
GENERAL DESCRIPTION

The DS21Q59 E1 quad transceiver contains all the necessary functions for connecting to four E1 lines. The DS21Q59 is a direct replacement for the DS21Q50, with the addition of signaling access and improved interrupt handling. It is composed of a line interface unit (LIU), framer, and a TDM backplane interface, and is controlled through an 8-bit parallel port configured for Intel or Motorola bus operations or serial port operation.

APPLICATIONS

DSLAMs
Routers
IMA and WAN Equipment

PIN CONFIGURATION



FEATURES

- Four Complete E1 (CEPT) PCM-30/ISDN-PRI Transceivers
- Pin Compatible with the DS21Q50
- Long-Haul and Short-Haul Line Interfaces
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Frames to FAS, CAS, and CRC4 Formats
- CAS/CCS Signaling Support
- 4MHz/8MHz/16MHz Clock Synthesizer
- Flexible System Clock with Automatic Source Switching on Loss-of-Clock Source
- Two-Frame Elastic-Store Slip Buffer on the Receive Side
- Interleaving PCM Bus Operation Up to 16.384MHz
- Configurable Parallel and Serial Port Operation
- Detects and Generates Remote and AIS Alarms
- Fully Independent Transmit and Receive Functionality
- Four Separate Loopback Functions
- PRBS Generation/Detection/Error Counting
- 3.3V Low-Power CMOS
- Large Counters for Bipolar and Code Violations, CRC4 Codeword Errors, FAS Word Errors, and E Bits
- Eight Additional User-Configurable Output Pins
- 100-Pin (14mm) LQFP Package

ORDERING INFORMATION

| PART | TEMP RANGE | PIN-PACKAGE |
|-----------|----------------|-------------|
| DS21Q59L | 0°C to +70°C | 100 LQFP |
| DS21Q59LN | -40°C to +85°C | 100 LQFP |

Note: Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.

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1. ACRONYMS

The following abbreviations are used throughout this data sheet:

| | |
|-------|---|
| FAS | Frame Alignment Signal |
| CAS | Channel Associated Signaling |
| MF | Multiframe |
| Si | International Bits |
| CRC4 | Cyclical Redundancy Check |
| CCS | Common Channel Signaling |
| Sa | Additional bits |
| E-Bit | CRC4 Error Bits |
| LOC | Loss of Clock |
| TCLK | This generally refers to the transmit rate clock and can reference an actual input signal to the device (TCLK) or an internally derived signal used for transmission. |
| RCLK | This generally refers to the recovered network clock and can be a reference to an actual output signal from the device or an internal signal. |

2. DETAILED DESCRIPTION

The LIU is composed of a transmit interface, receive interface, and a jitter attenuator. The transmit interface generates the necessary waveshapes for driving the network, depending on the type of media used. E1 waveform generation includes G.703 waveshapes for both 75Ω coax and 120Ω twisted cables. The receive interface recovers clock and data from the network. The receive sensitivity adjusts automatically to the incoming signal. The jitter attenuator removes phase jitter from the transmitted or received signal. The crystal-less jitter attenuator only requires a 2.048MHz MCLK and can be placed in either the transmit or receive data paths. An additional feature of the LIU is a code mark inversion (CMI) coder/decoder for interfacing to optical networks.

On the transmit side, the backplane interface section provides clock/data and frame-sync signals to the framer. The framer inserts the appropriate synchronization framing patterns, alarm information, calculates and inserts the CRC codes, and provides the HDB3 (zero code suppression) and alternate mark inversion (AMI) line coding. The receive-side framer decodes AMI and HDB3 line coding, synchronizes to the data stream, reports alarm information, counts framing/coding/CRC errors, and provides clock/data and frame-sync signals to the backplane interface section.

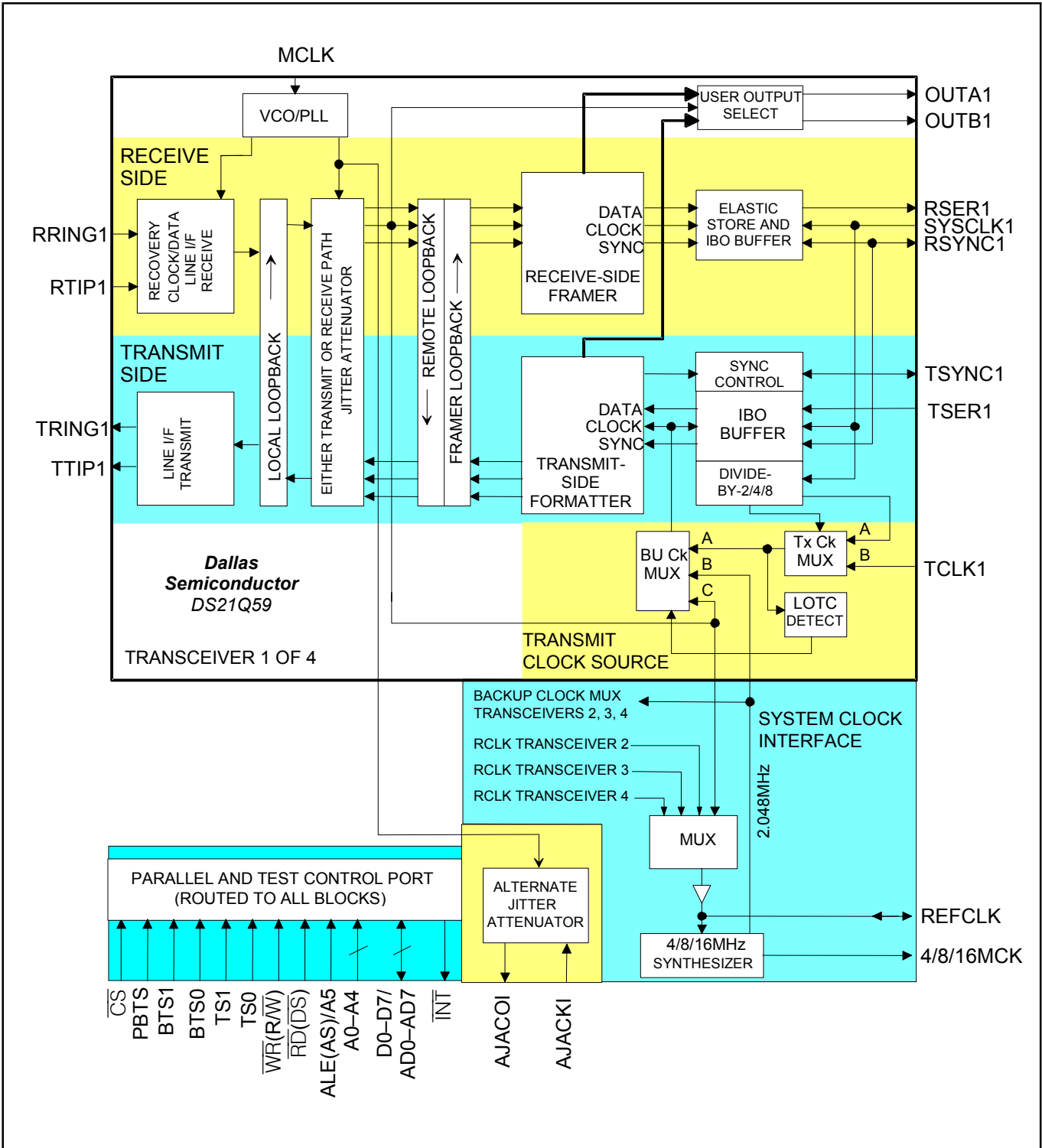
The backplane interface provides a versatile method of sending and receiving data from the host system. The receive elastic store provides a method for interfacing to asynchronous systems. The elastic store also manages slip conditions (asynchronous interface). An interleave bus option (IBO) is provided to allow multiple E1 lines to share a high-speed backplane.

The parallel port provides access for control and configuration of all the DS21Q59's features. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection. The device fully meets all the latest E1 specifications, including ITU-T G.703, G.704, G.706, G.823, G.732 and I.431 ETS 300 011, ETS 300 233, and ETS 300 166 as well as CTR12 and CTR4.

The DS21Q59 is optimized for high-density termination of E1 lines. Two significant features are included for this type of application: the IBO and a system clock synthesizer feature. The IBO allows up to eight E1 data streams to be multiplexed onto a single high-speed PCM bus without additional external logic. The system clock synthesizer allows any of the E1 lines to be selected as the master source of the clock for the system and for all the transmitters. This is also accomplished without the need of external logic. Each of the four transceivers has a clock and data jitter attenuator that can be assigned to either the transmit or receive path. In addition there is a single, undedicated clock jitter attenuator that can be hardware configured as needed by the user. Each transceiver also contains a PRBS pattern generator and detector. [Figure 23-1](#) shows a simplified typical application that terminates eight E1 lines (transmit and receive pairs) and combines the data into a single 16.384MHz PCM bus. The 16.384MHz system clock is derived and phase-locked to one of the eight E1 lines. On the receive side of each port, an elastic store provides logical management of any slip conditions due to the asynchronous relationship of the eight E1 lines. In this application all eight transmitters are timed to the selected E1 line.

3. BLOCK DIAGRAM

Figure 3-1. Block Diagram



4. PIN DESCRIPTION

Table 4-A. Pin Description (Sorted by Function)

| PIN | NAME | | TYPE | FUNCTION [SERIAL PORT MODE IN BRACKETS] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 71 | 4/8/16MCK | — | O | 4.096MHz, 8.192MHz, or 16.384MHz Clock |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input-Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output-Clock Edge Select] |
| 47 | A2 | — | I | Address Bus Bit 2 |
| 48 | A3 | — | I | Address Bus Bit 3 |
| 49 | A4 | — | I | Address Bus Bit 4 |
| 70 | AJACKI | — | I | Alternate Jitter Attenuator Clock Input |
| 69 | AJACKO | — | O | Alternate Jitter Attenuator Clock Output |
| 50 | ALE (AS)/A5 | — | I | Address Latch Enable/Address Bus Bit 5 |
| 96 | BTS0 | — | | Bus Type Select 0 |
| 97 | BTS1 | — | | Bus Type Select 1 |
| 98 | CS | — | I | Chip Select |
| 19 | D0/AD0 | — | I/O | Data Bus Bit 0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | — | I/O | Data Bus Bit 1/Address/Data Bus Bit 1 |
| 21 | D2/AD2 | — | I/O | Data Bus Bit 2/Address/Data Bus Bit 2 |
| 22 | D3/AD3 | — | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | — | I/O | Data Bus Bit 4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | — | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | — | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output] |
| 84 | DVDD1 | — | — | Digital Positive Supply |
| 59 | DVDD2 | — | — | Digital Positive Supply |
| 34 | DVDD3 | — | — | Digital Positive Supply |
| 9 | DVDD4 | — | — | Digital Positive Supply |
| 83 | DVSS1 | — | — | Digital Signal Ground |
| 58 | DVSS2 | — | — | Digital Signal Ground |
| 33 | DVSS3 | — | — | Digital Signal Ground |
| 8 | DVSS4 | — | — | Digital Signal Ground |
| 94 | INT | — | O | Interrupt |
| 73 | MCLK | — | I | Master Clock Input |
| 61 | OUTA1 | — | O | User-Selectable Output A |
| 36 | OUTA2 | — | O | User-Selectable Output A |
| 11 | OUTA3 | — | O | User-Selectable Output A |
| 86 | OUTA4 | — | O | User-Selectable Output A |
| 60 | OUTB1 | — | O | User-Selectable Output B |
| 35 | OUTB2 | — | O | User-Selectable Output B |
| 10 | OUTB3 | — | O | User-Selectable Output B |
| 85 | OUTB4 | — | O | User-Selectable Output B |
| 95 | PBTS | — | I | Parallel Bus Type Select |
| 75 | RD (DS) | SCLK | I | Read Input (Data Strobe) [Serial Port Clock] |
| 72 | REFCLK | — | I/O | Reference Clock |
| 67 | RRING1 | — | I | Receive Analog Ring Input |
| 42 | RRING2 | — | I | Receive Analog Ring Input |
| 17 | RRING3 | — | I | Receive Analog Ring Input |
| 92 | RRING4 | — | I | Receive Analog Ring Input |
| 63 | RSER1 | — | O | Receive Serial Data |
| 38 | RSER2 | — | O | Receive Serial Data |
| 13 | RSER3 | — | O | Receive Serial Data |
| 88 | RSER4 | — | O | Receive Serial Data |
| 64 | RSYNC1 | — | I/O | Receive Sync |
| 39 | RSYNC2 | — | I/O | Receive Sync |
| 14 | RSYNC3 | — | I/O | Receive Sync |

| PIN | NAME | | TYPE | FUNCTION [SERIAL PORT MODE IN BRACKETS] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 89 | RSYNC4 | — | I/O | Receive Sync |
| 66 | RTIP1 | — | I | Receive Analog Tip Input |
| 41 | RTIP2 | — | I | Receive Analog Tip Input |
| 16 | RTIP3 | — | I | Receive Analog Tip Input |
| 91 | RTIP4 | — | I | Receive Analog Tip Input |
| 93 | RVDD1 | — | — | Receive Analog Positive Supply |
| 68 | RVDD2 | — | — | Receive Analog Positive Supply |
| 43 | RVDD3 | — | — | Receive Analog Positive Supply |
| 18 | RVDD4 | — | — | Receive Analog Positive Supply |
| 90 | RVSS1 | — | — | Receive Analog Signal Ground |
| 65 | RVSS2 | — | — | Receive Analog Signal Ground |
| 40 | RVSS3 | — | — | Receive Analog Signal Ground |
| 15 | RVSS4 | — | — | Receive Analog Signal Ground |
| 62 | SYSCLK1 | — | I | Transmit/Receive System Clock |
| 37 | SYSCLK2 | — | I | Transmit/Receive System Clock |
| 12 | SYSCLK3 | — | I | Transmit/Receive System Clock |
| 87 | SYSCLK4 | — | I | Transmit/Receive System Clock |
| 80 | TCLK1 | — | I | Transmit Clock |
| 55 | TCLK2 | — | I | Transmit Clock |
| 30 | TCLK3 | — | I | Transmit Clock |
| 5 | TCLK4 | — | I | Transmit Clock |
| 79 | TRING1 | — | O | Transmit Analog Ring Output |
| 54 | TRING2 | — | O | Transmit Analog Ring Output |
| 29 | TRING3 | — | O | Transmit Analog Ring Output |
| 4 | TRING4 | — | O | Transmit Analog Ring Output |
| 99 | TS0 | — | I | Transceiver Select 0 |
| 100 | TS1 | — | I | Transceiver Select 1 |
| 81 | TSER1 | — | I | Transmit Serial Data |
| 56 | TSER2 | — | I | Transmit Serial Data |
| 31 | TSER3 | — | I | Transmit Serial Data |
| 6 | TSER4 | — | I | Transmit Serial Data |
| 82 | TSYNC1 | — | I/O | Transmit Sync |
| 57 | TSYNC2 | — | I/O | Transmit Sync |
| 32 | TSYNC3 | — | I/O | Transmit Sync |
| 7 | TSYNC4 | — | I/O | Transmit Sync |
| 76 | TTIP1 | — | O | Transmit Analog Tip Output |
| 51 | TTIP2 | — | O | Transmit Analog Tip Output |
| 26 | TTIP3 | — | O | Transmit Analog Tip Output |
| 1 | TTIP4 | — | O | Transmit Analog Tip Output |
| 78 | TVDD1 | — | — | Transmit Analog Positive Supply |
| 53 | TVDD2 | — | — | Transmit Analog Positive Supply |
| 28 | TVDD3 | — | — | Transmit Analog Positive Supply |
| 3 | TVDD4 | — | — | Transmit Analog Positive Supply |
| 77 | TVSS1 | — | — | Transmit Analog Signal Ground |
| 52 | TVSS2 | — | — | Transmit Analog Signal Ground |
| 27 | TVSS3 | — | — | Transmit Analog Signal Ground |
| 2 | TVSS4 | — | — | Transmit Analog Signal Ground |
| 74 | WR (R/W) | SDI | I | Write Input (Read/Write) [Serial Data Input] |

Note: EQVSS lines are wired to RVSS lines.

Table 4-B. Pin Assignments (Sorted by Number)

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 1 | TTIP4 | — | O | Transmit Analog Tip Output |
| 2 | TVSS4 | — | — | Transmit Analog Signal Ground |
| 3 | TVDD4 | — | — | Transmit Analog Positive Supply |
| 4 | TRING4 | — | O | Transmit Analog Ring Output |
| 5 | TCLK4 | — | I | Transmit Clock |
| 6 | TSER4 | — | I | Transmit Serial Data |
| 7 | TSYNC4 | — | I/O | Transmit Sync |
| 8 | DVSS4 | — | — | Digital Signal Ground |
| 9 | DVDD4 | — | — | Digital Positive Supply |
| 10 | OUTB3 | — | O | User-Selectable Output B |
| 11 | OUTA3 | — | O | User-Selectable Output A |
| 12 | SYSCLK3 | — | I | Transmit/Receive System Clock |
| 13 | RSER3 | — | O | Receive Serial Data |
| 14 | RSYNC3 | — | I/O | Receive Sync |
| 15 | RVSS4 | — | — | Receive Analog Signal Ground |
| 16 | RTIP3 | — | I | Receive Analog Tip Input |
| 17 | RRING3 | — | I | Receive Analog Ring Input |
| 18 | RVDD4 | — | — | Receive Analog Positive Supply |
| 19 | D0/AD0 | — | I/O | Data Bus Bit 0/Address/Data Bus Bit 0 |
| 20 | D1/AD1 | — | I/O | Data Bus Bit 1/Address/Data Bus Bit 1 |
| 21 | D2/AD2 | — | I/O | Data Bus Bit 2/Address/Data Bus Bit 2 |
| 22 | D3/AD3 | — | I/O | Data Bus Bit 3/Address/Data Bus Bit 3 |
| 23 | D4/AD4 | — | I/O | Data Bus Bit 4/Address/Data Bus Bit 4 |
| 24 | D5/AD5 | — | I/O | Data Bus Bit 5/Address/Data Bus Bit 5 |
| 25 | D6/AD6 | — | I/O | Data Bus Bit 6/Address/Data Bus Bit 6 |
| 26 | TTIP3 | — | O | Transmit Analog Tip Output |
| 27 | TVSS3 | — | — | Transmit Analog Signal Ground |
| 28 | TVDD3 | — | — | Transmit Analog Positive Supply |
| 29 | TRING3 | — | O | Transmit Analog Ring Output |
| 30 | TCLK3 | — | I | Transmit Clock |
| 31 | TSER3 | — | I | Transmit Serial Data |
| 32 | TSYNC3 | — | I/O | Transmit Sync |
| 33 | DVSS3 | — | — | Digital Signal Ground |
| 34 | DVDD3 | — | — | Digital Positive Supply |
| 35 | OUTB2 | — | O | User-Selectable Output B |
| 36 | OUTA2 | — | O | User-Selectable Output A |
| 37 | SYSCLK2 | — | I | Transmit/Receive System Clock |
| 38 | RSER2 | — | O | Receive Serial Data |
| 39 | RSYNC2 | — | I/O | Receive Sync |
| 40 | RVSS3 | — | — | Receive Analog Signal Ground |
| 41 | RTIP2 | — | I | Receive Analog Tip Input |
| 42 | RRING2 | — | I | Receive Analog Ring Input |
| 43 | RVDD3 | — | — | Receive Analog Positive Supply |
| 44 | D7/AD7 | SDO | I/O | Data Bus Bit 7/Address/Data Bus Bit 7 [Serial Data Output] |
| 45 | A0 | ICES | I | Address Bus Bit 0/Serial Port [Input-Clock Edge Select] |
| 46 | A1 | OCES | I | Address Bus Bit 1/Serial Port [Output-Clock Edge Select] |
| 47 | A2 | — | I | Address Bus Bit 2 |
| 48 | A3 | — | I | Address Bus Bit 3 |
| 49 | A4 | — | I | Address Bus Bit 4 |
| 50 | ALE (AS)/A5 | — | I | Address Latch Enable/Address Bus Bit 5 |
| 51 | TTIP2 | — | O | Transmit Analog Tip Output |
| 52 | TVSS2 | — | — | Transmit Analog Signal Ground |
| 53 | TVDD2 | — | — | Transmit Analog Positive Supply |
| 54 | TRING2 | — | O | Transmit Analog Ring Output |

| PIN | NAME | | TYPE | FUNCTION [Serial Port Mode in Brackets] |
|-----|--------------------------|------------------------|------|--|
| | PARALLEL PORT ENABLED | SERIAL PORT ENABLED | | |
| 55 | TCLK2 | — | I | Transmit Clock |
| 56 | TSER2 | — | I | Transmit Serial Data |
| 57 | TSYNC2 | — | I/O | Transmit Sync |
| 58 | DVSS2 | — | — | Digital Signal Ground |
| 59 | DVDD2 | — | — | Digital Positive Supply |
| 60 | OUTB1 | — | O | User-Selectable Output B |
| 61 | OUTA1 | — | O | User-Selectable Output A |
| 62 | SYSCLK1 | — | I | Transmit/Receive System Clock |
| 63 | RSER1 | — | O | Receive Serial Data |
| 64 | RSYNC1 | — | I/O | Receive Sync |
| 65 | RVSS2 | — | — | Receive Analog Signal Ground |
| 66 | RTIP1 | — | I | Receive Analog Tip Input |
| 67 | RRING1 | — | I | Receive Analog Ring Input |
| 68 | RVDD2 | — | — | Receive Analog Positive Supply |
| 69 | AJACKO | — | O | Alternate Jitter Attenuator Clock Output |
| 70 | AJACKI | — | I | Alternate Jitter Attenuator Clock Input |
| 71 | 4/8/16MCK | — | O | 4.096MHz, 8.192MHz, or 16.384MHz Clock |
| 72 | REFCLK | — | I/O | Reference Clock |
| 73 | MCLK | — | I | Master Clock Input |
| 74 | \overline{WR} (R/W) | SDI | I | Write Input (Read/Write) [Serial Data Input] |
| 75 | \overline{RD} (DS) | SCLK | I | Read Input (Data Strobe) [Serial Port Clock] |
| 76 | TTIP1 | — | O | Transmit Analog Tip Output |
| 77 | TVSS1 | — | — | Transmit Analog Signal Ground |
| 78 | TVDD1 | — | — | Transmit Analog Positive Supply |
| 79 | TRING1 | — | O | Transmit Analog Ring Output |
| 80 | TCLK1 | — | I | Transmit Clock |
| 81 | TSER1 | — | I | Transmit Serial Data |
| 82 | TSYNC1 | — | I/O | Transmit Sync |
| 83 | DVSS1 | — | — | Digital Signal Ground |
| 84 | DVDD1 | — | — | Digital Positive Supply |
| 85 | OUTB4 | — | O | User-Selectable Output B |
| 86 | OUTA4 | — | O | User-Selectable Output A |
| 87 | SYSCLK4 | — | I | Transmit/Receive System Clock |
| 88 | RSER4 | — | O | Receive Serial Data |
| 89 | RSYNC4 | — | I/O | Receive Sync |
| 90 | RVSS1 | — | — | Receive Analog Signal Ground |
| 91 | RTIP4 | — | I | Receive Analog Tip Input |
| 92 | RRING4 | — | I | Receive Analog Ring Input |
| 93 | RVDD1 | — | — | Receive Analog Positive Supply |
| 94 | \overline{INT} | — | O | Interrupt |
| 95 | PBTS | — | I | Parallel Bus Type Select |
| 96 | BTS0 | — | — | Bus Type Select 0 |
| 97 | BTS1 | — | — | Bus Type Select 1 |
| 98 | CS | — | I | Chip Select |
| 99 | TS0 | — | I | Transceiver Select 0 |
| 100 | TS1 | — | I | Transceiver Select 1 |

Note: EQVSS lines are wired to RVSS.

4.1 Pin Function Descriptions

Table 4-C. System (Backplane) Interface Pins

| NAME | TYPE | FUNCTION |
|--------|------|---|
| TCLK | I | Transmit Clock. TCLK is a 2.048MHz primary clock that is used to clock data through the transmit formatter. |
| TSER | I | Transmit Serial Data. Transmit NRZ serial data. TSER is sampled on the falling edge of TCLK when IBO disabled. It is sampled on the falling edge of SYSCLK when the IBO function is enabled. |
| TSYNC | I/O | Transmit Sync. As an input, pulse at this pin establishes either frame or multiframe boundaries for the transmitter. As an output, it can be programmed to output either a frame or multiframe pulse. |
| RSER | O | Receive Serial Data. RSER is the received NRZ serial data. RSER is updated on the rising edges of RCLK when the receive elastic store is disabled. It is updated on the rising edges of SYSCLK when the receive elastic store is enabled. |
| RSYNC | I/O | Receive Sync. An extracted pulse one RCLK wide is output at this pin that identifies either frame or CAS/CRC4 multiframe boundaries. If the receive elastic store is enabled, this pin can be enabled to be an input at which a frame-boundary pulse synchronous with SYSCLK is applied. |
| SYSCLK | I | System Clock. SYSCLK is a 2.048MHz clock used to clock data out of the receive elastic store. When the IBO is enabled SYSCLK can be a 4.096MHz, 8.192MHz, or 16.384MHz clock. |
| OUTA | O | User-Selectable Output A. OUTA is a multifunction pin the host can program to output various alarms, clocks, or data, or be used to control external circuitry. |
| OUTB | O | User-Selectable Output B. OUTB is a multifunction pin the host can program to output various alarms, clocks, or data, or be used to control external circuitry. |

Table 4-D. Alternate Jitter Attenuator

| NAME | TYPE | FUNCTION |
|--------|------|---|
| AJACKI | I | Alternate Jitter Attenuator Clock Input. AJACKI is clock input to the alternate jitter attenuator. |
| AJACKO | O | Alternate Jitter Attenuator Clock Output. AJACKO is clock output of the alternate jitter attenuator. |

Table 4-E. Clock Synthesizer

| NAME | TYPE | FUNCTION |
|-----------|------|---|
| 4/8/16MCK | O | 4.096MHz/8.192MHz/16.384MHz Clock Output. 4/8/16MCK is a 4.096MHz, 8.192MHz, or 16.384MHz clock output that is referenced to one of the four recovered line clocks (RCLKs) or to an external 2.048MHz reference. |
| REFCLK | I/O | Reference Clock. REFCLK can be configured as an output to source a 2.048MHz reference clock or as an input to supply a 2.048MHz reference clock from an external source to the clock synthesizer. |

Table 4-F. Parallel Port Control Pins

| NAME | TYPE | FUNCTION |
|--|------|---|
| $\overline{\text{INT}}$ | O | Interrupt. $\overline{\text{INT}}$ flags the host controller during conditions and change of conditions defined in status registers 1 and 2 and the HDLC status register. It is an active-low, open-drain output. |
| BTS0 | I | Bus Type Select Bit 0. BTS0 is used with BTS1 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode. |
| BTS1 | I | Bus Type Select Bit 1. BTS1 is used with BTS0 to select between muxed, nonmuxed, serial bus operation, and output high-Z mode. |
| TS0 | I | Transceiver Select Bit 0. TS0 is used with TS1 to select one of four transceivers. |
| TS1 | I | Transceiver Select Bit 1. TS1 is used with TS0 to select one of four transceivers. |
| PBTS | I | Parallel Bus Type Select. PBTS is used to select between Motorola and Intel parallel bus types. |
| AD0 to AD7/SDO | I/O | Data Bus or Address/Data Bus [D0 to D6], Data Bus or Address/Data Bus [D7]/Serial Port Output. In nonmultiplexed bus operation (MUX = 0), these pins serve as the data bus. In multiplexed bus operation (MUX = 1), they serve as an 8-bit multiplexed address/data bus. |
| A0 to A4 | I | Address Bus. In nonmultiplexed bus operation, these pins serve as the address bus. In multiplexed bus operation, these pins are not used and should be wired low. |
| $\overline{\text{RD}}$ ($\overline{\text{DS}}$)/SCLK | I | Read Input—Data Strobe/Serial Port Clock. $\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals. DS is active high when in multiplexed mode (Section 26). |
| $\overline{\text{CS}}$ | I | Chip Select. $\overline{\text{CS}}$ must be low to read or write to the device. It is an active-low signal. |
| ALE (AS)/A5 | I | Address Latch Enable (Address Strobe) or A6. In nonmultiplexed bus operation, this pin serves as the upper address bit. In multiplexed bus operation, it demultiplexes the bus on a positive-going edge. |
| $\overline{\text{WR}}$ ($\overline{\text{RW}}$)/SDI | I | Write Input (Read/Write)/Serial Port Data Input, Active Low |

Table 4-G. Serial Port Control Pins

| NAME | TYPE | FUNCTION |
|------|------|---|
| SDO | O | Serial Port Data Output. Data at this output can be updated on the rising or falling edge of SCLK. |
| SDI | I | Serial Port Data Input. Data at this input can be sampled on the rising or falling edge of SCLK. |
| ICES | I | Input Clock-Edge Select. ICES is used to select which SCLK clock edge samples data at SDI. |
| OCES | I | Output Clock-Edge Select. OCES is used to select which SCLK clock edge updates data at SDO. |
| SCLK | I | Serial Port Clock. SCLK is used to clock data into and out of the serial port. |

Table 4-H. Line Interface Pins

| NAME | TYPE | FUNCTION |
|----------------|------|---|
| MCLK | I | Master Clock Input. A 2.048MHz (± 50 ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. |
| RTIP and RRING | I | Receive Tip and Ring. RTIP and RRING are analog inputs for clock recovery circuitry. These pins connect through a 1:1 step-up transformer to the E1 line. See Section 21 for details. |
| TTIP and TRING | O | Transmit Tip and Ring. TTIP and TRING are analog line-driver outputs. These pins connect through a 1:2 step-up transformer to the E1 line. See Section 21 for details. |

Table 4-I. Supply Pins

| NAME | TYPE | FUNCTION |
|------|--------|---|
| DVDD | Supply | Digital Positive Supply. 3.3V $\pm 5\%$. Should be wired to the RVDD and TVDD pins. |
| RVDD | Supply | Receive Analog Positive Supply. 3.3V $\pm 5\%$. Should be wired to the DVDD and TVDD pins. |
| TVDD | Supply | Transmit Analog Positive Supply. 3.3V $\pm 5\%$. Should be wired to the RVDD and DVDD pins. |
| DVSS | Supply | Digital Signal Ground. 0V. Should be wired to the RVSS and TVSS pins. |
| RVSS | Supply | Receive Analog Signal Ground. 0V. Should be wired to DVSS and TVSS. |
| TVSS | Supply | Transmit Analog Signal Ground. 0V. Should be wired to DVSS and RVSS. |

5. FUNCTIONAL DESCRIPTION

The analog AMI/HDB3 waveform off the E1 line is transformer-coupled into the DS21Q59's RRING and RTIP pins. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive framer, where the digital serial stream is analyzed to locate the framing/multiframe pattern. The DS21Q59 contains an active filter that reconstructs the analog-received signal for the nonlinear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -43dB, which allows the device to operate on cables over 2km in length. The receive framer locates FAS frame and CRC and CAS multiframe boundaries as well as detects incoming alarms including carrier loss, loss of synchronization, AIS, and remote alarm. If needed, the receive elastic store can be enabled to absorb the phase and frequency differences between the recovered E1 data stream and an asynchronous backplane clock, which is provided at the SYSCLK input. The clock applied at the SYSCLK input can be either a 2.048MHz/4.096MHz/8.192MHz or 16.384MHz clock. The transmit framer is independent of the receive framer in both the clock requirements and characteristics. The transmit formatter provides the necessary frame/multiframe data overhead for E1 transmission.

Note: This data sheet assumes a particular nomenclature of the E1 operating environment. In each 125 μ s frame, there are 32 8-bit time slots numbered 0 to 31. Time slot 0 is transmitted first and received first. These 32 time slots are also referred to as channels with a numbering scheme of 1 to 32. Time slot 0 is identical to channel 1, time slot 1 is identical to channel 2, and so on. Each time slot (or channel) is made up of eight bits that are numbered 1 to 8. Bit number 1, MSB, is transmitted first. Bit number 8, the LSB, is transmitted last. The term "locked" is used to refer to two clock signals that are phase-locked or frequency-locked or derived from a common clock (i.e., an 8.192MHz clock can be locked to a 2.048MHz clock if they share the same 8kHz component).

6. HOST INTERFACE PORT

The DS21Q59 is controlled through either a nonmultiplexed bus, a multiplexed bus, or serial interface bus by an external microcontroller or microprocessor. The device can operate with either Intel or Motorola bus timing configurations. See [Table 6-A](#) for a description of the bus configurations. Motorola bus signals are listed in parentheses (). See the timing diagrams in the *AC Electrical Characteristics* in Section [26](#) for more details.

Table 6-A. Bus Mode Select

| PBTS | BTS1 | BTS0 | PARALLEL PORT MODE |
|------|------|------|-------------------------|
| 0 | 0 | 0 | Intel Multiplexed |
| 0 | 0 | 1 | Intel Nonmultiplexed |
| 1 | 0 | 0 | Motorola Multiplexed |
| 1 | 0 | 1 | Motorola Nonmultiplexed |
| X | 1 | 0 | Serial |
| X | 1 | 1 | TEST (Outputs High-Z) |

6.1 Parallel Port Operation

When using the parallel interface on the DS21Q59 (BTS1 = 0) the user has the option for either multiplexed bus operation (BTS1 = 0, BTS0 = 0) or nonmultiplexed bus operation (BTS1 = 0, BTS0 = 1). The DS21Q59 can operate with either Intel or Motorola bus timing configurations. If the PBTS pin is wired low, Intel timing is selected; if wired high, Motorola timing is selected. All Motorola bus signals are listed in parentheses (). See the timing diagrams in Section [26](#) for more details.

6.2 Serial Port Operation

Setting the BTS1 pin = 1 and BTS0 pin = 0 enables the serial bus interface on the DS21Q59. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous reads or writes by the host. See Section [26](#) for the AC timing of the serial port. All serial port accesses are LSB first. See [Figure 6-1](#), [Figure 6-2](#), [Figure 6-3](#), and [Figure 6-4](#) for more details.

Reading or writing to the internal registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command byte specifies whether the access is a read (1) or a write (0). The next five bits identify the register address. The next bit is reserved and must be set to 0 for proper operation. The last bit (MSB) of the address/command byte enables the burst mode when set to 1. The burst mode causes all registers to be consecutively written or read.

All data transfers are initiated by driving the \overline{CS} input low. When input-clock edge select (ICES) is low, input data is latched on the rising edge of SCLK; when ICES is high, input data is latched on the falling edge of SCLK. When output-clock edge select (OCES) is low, data is output on the falling edge of SCLK; when OCES is high, data is output on the rising edge of SCLK. Data is held until the next falling or rising edge. All data transfers are terminated if the \overline{CS} input transitions high. Port control logic is disabled and SDO is tri-stated when \overline{CS} is high.

Figure 6-1. Serial Port Operation Mode 1

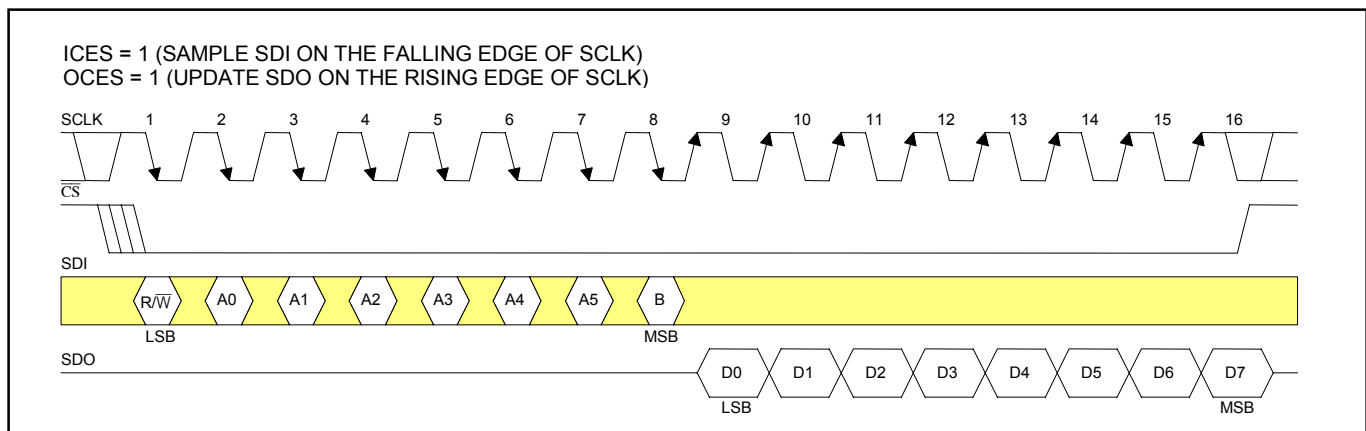


Figure 6-2. Serial Port Operation Mode 2

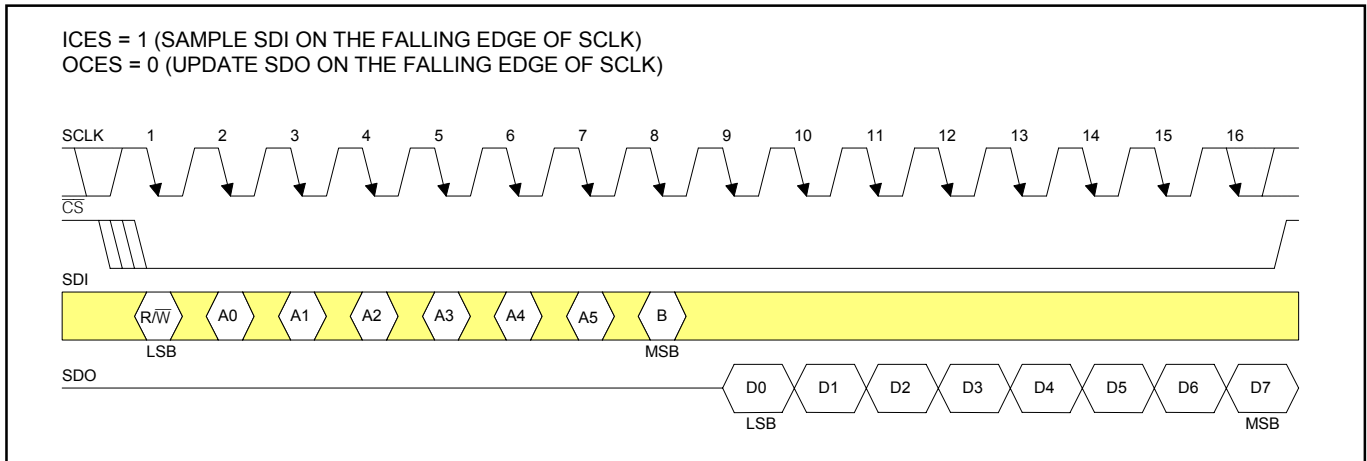


Figure 6-3. Serial Port Operation Mode 3

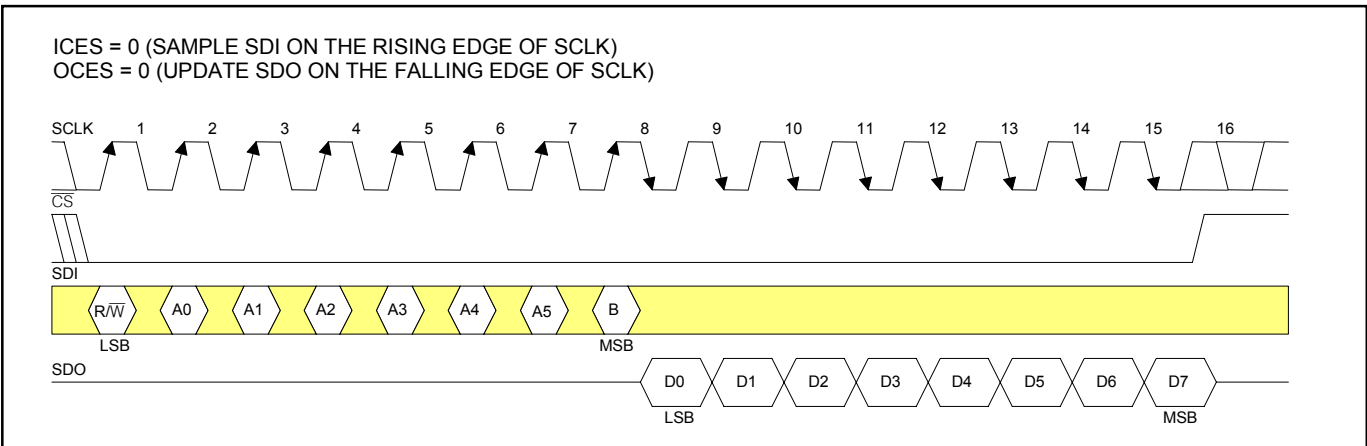
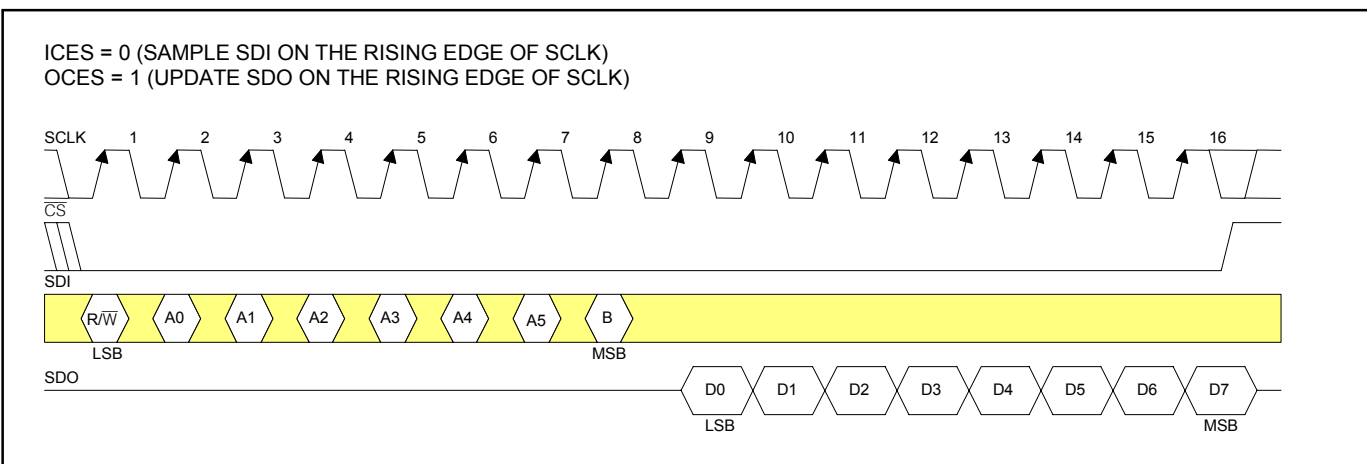


Figure 6-4. Serial Port Operation Mode 4



7. REGISTER MAP

Table 7-A. Register Map (Sorted by Address)

| ADDRESS | R/W | NAME | FUNCTION |
|---------|-----|--------------------|--|
| 00 | R | VCR1 | BPV or Code Violation Count 1 |
| 01 | R | VCR2 | BPV or Code Violation Count 2 |
| 02 | R | CRCCR1 | CRC4 Error Count 1 |
| 03 | R | CRCCR2 | CRC4 Error Count 2 |
| 04 | R | EBCR1 | E-Bit Count 1/PRBS Error Count 1 |
| 05 | R | EBCR2 | E-Bit Count 2/PRBS Error Count 2 |
| 06 | R | FASCR1 | FAS Error Count 1 |
| 07 | R | FASCR2 | FAS Error Count 2 |
| 08 | R/W | RIR | Receive Information |
| 09 | R | SSR | Synchronizer Status |
| 0A | R/W | SR1 | Status 1 |
| 0B | R/W | SR2 | Status 2 |
| 0C | — | — | Unused |
| 0D | — | — | Unused |
| 0E | — | — | Unused |
| 0F | R | IDR | Device ID (Note 1) |
| 10 | R/W | RCR | Receive Control |
| 11 | R/W | TCR | Transmit Control 1 |
| 12 | R/W | CCR1 | Common Control 1 |
| 13 | R/W | CCR2 | Common Control 2 |
| 14 | R/W | CCR3 | Common Control 3 |
| 15 | R/W | CCR4 | Common Control 4 |
| 16 | R/W | CCR5 | Common Control 5 |
| 17 | R/W | LICR | Line Interface Control Register |
| 18 | R/W | IMR1 | Interrupt Mask 1 |
| 19 | R/W | IMR2 | Interrupt Mask 2 |
| 1A | R/W | OUTAC | Output A Control |
| 1B | R/W | OUTBC | Output B Control |
| 1C | R/W | IBO | Interleave Bus Operation Register |
| 1D | R/W | SCICR | System Clock-Interface Control Register (Note 1) |
| 1E | R/W | TEST3 (set to 00h) | Test 2 (Note 2) |
| 1F | R/W | CCR7 | Common Control 7 |
| 20 | R/W | TAF | Transmit Align Frame |
| 21 | R/W | TNAF | Transmit Nonalign Frame |
| 22 | R | TDS0M | Transmit DS0 Monitor |
| 23 | R/W | TIDR | Transmit Idle Definition |
| 24 | R/W | TIR1 | Transmit Idle 1 |
| 25 | R/W | TIR2 | Transmit Idle 2 |
| 26 | R/W | TIR3 | Transmit Idle 3 |
| 27 | R/W | TIR4 | Transmit Idle 4 |
| 28 | R | RAF | Receive Align Frame |
| 29 | R | RNAF | Receive Nonalign Frame |
| 2A | R | RDS0M | Receive DS0 Monitor |
| 2B | R/W | PCLB1 | Per-Channel Loopback Control 1 |
| 2C | R/W | PCLB2 | Per-Channel Loopback Control 2 |
| 2D | R/W | PCLB3 | Per-Channel Loopback Control 3 |
| 2E | R/W | PCLB4 | Per-Channel Loopback Control 4 |
| 2F | R/W | CCR6 | Common Control 6 |
| 30 | R/W | SA1 | Signaling Access Register 1 |
| 31 | R/W | SA2 | Signaling Access Register 2 |
| 32 | R/W | SA3 | Signaling Access Register 3 |
| 33 | R/W | SA4 | Signaling Access Register 4 |
| 34 | R/W | SA5 | Signaling Access Register 5 |
| 35 | R/W | SA6 | Signaling Access Register 6 |
| 36 | R/W | SA7 | Signaling Access Register 7 |

| ADDRESS | R/W | NAME | FUNCTION |
|---------|-----|------|------------------------------|
| 37 | R/W | SA8 | Signaling Access Register 8 |
| 38 | R/W | SA9 | Signaling Access Register 9 |
| 39 | R/W | SA10 | Signaling Access Register 10 |
| 3A | R/W | SA11 | Signaling Access Register 11 |
| 3B | R/W | SA12 | Signaling Access Register 12 |
| 3C | R/W | SA13 | Signaling Access Register 13 |
| 3D | R/W | SA14 | Signaling Access Register 14 |
| 3E | R/W | SA15 | Signaling Access Register 15 |
| 3F | R/W | SA16 | Signaling Access Register 16 |

Note 1: The device ID register and the system clock-interface control register exist in Transceiver 1 only (TS0, TS1 = 0).

Note 2: Only the factory uses the test register; this register must be cleared (set to all zeros) on power-up initialization to ensure proper operation.

8. CONTROL, ID, AND TEST REGISTERS

The DS21Q59 operation is configured through a set of nine control registers. Typically, registers are only accessed when the system is first powered up. Once the device has been initialized, the control registers only need to be accessed when there is a change in the system configuration. There is one receive control register (RCR), one transmit control register (TCR), and seven common control registers (CCR1 to CCR7). Each of these registers is described in this section.

Address 0Fh has a device identification register (IDR). The four MSBs of this read-only register are fixed to 1 0 0 1, indicating that a DS21Q59 E1 quad transceiver is present. The lower 4 bits of the IDR are used to identify the revision of the device. This register exists in Transceiver 1 only (TS0, TS1 = 0).

The factory in testing the DS21Q59 uses the test register at addresses 1E. On power-up, the test register should be set to 00h for the DS21Q59 to properly operate.

Register Name: **IDR**
 Register Description: **Device Identification Register**
 Register Address: **0F Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|-----|-----|-----|-----|
| Name | 1 | 0 | 0 | 1 | ID3 | ID2 | ID1 | ID0 |

| NAME | BIT | FUNCTION |
|------|-----|--|
| 1 | 7 | Bit 7 |
| 0 | 6 | Bit 6 |
| 0 | 5 | Bit 5 |
| 1 | 4 | Bit 4 |
| ID3 | 3 | Chip Revision Bit 3. MSB of a decimal code that represents the chip revision. |
| ID2 | 1 | Chip Revision Bit 2 |
| ID1 | 2 | Chip Revision Bit 1 |
| ID0 | 0 | Chip Revision Bit 0. LSB of a decimal code that represents the chip revision. |

8.1 Power-Up Sequence

On power-up and after the supplies are stable, the DS21Q59 should be configured for operation by writing to all the internal registers (this includes setting the test register to 00h) since the contents of the internal registers cannot be predicted on power-up. The LIRST (CCR5.4) should be toggled from 0 to 1 to reset the line interface circuitry. (It takes the device about 40ms to recover from the LIRST bit being toggled.) After the SYSCLK input is stable, the ESR bits (CCR4.5 and CCR4.6) should be toggled from 0 to 1 (this step can be skipped if the elastic store is disabled).

Register Name: **RCR**
 Register Description: **Receive Control Register**
 Register Address: **10 Hex**

| | | | | | | | | |
|-------|------|-----|------|------|---|-----|-------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RSMF | RSM | RSIO | RESE | — | FRC | SYNCE | RESYNC |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| RSMF | 7 | RSYNC Multiframe Function. Only used if the RSYNC pin is programmed in the multiframe mode (RCR.6 = 1). 0 = RSYNC outputs CAS multiframe boundaries. 1 = RSYNC outputs CRC4 multiframe boundaries. |
| RSM | 6 | RSYNC Mode Select 0 = frame mode (see the timing diagrams in Section 24.1) 1 = multiframe mode (see the timing diagrams in Section 24.1) |
| RSIO | 5 | RSYNC I/O Select. (Note: This bit must be set to 0 when RCR .4 = 0.) 0 = RSYNC is an output (depends on RCR.6) 1 = RSYNC is an input (only valid if elastic store enabled) |
| RESE | 4 | Receive Elastic Store Enable 0 = elastic store is bypassed 1 = elastic store is enabled |
| — | 3 | Unused. Should be set = 0 for proper operation. |
| FRC | 2 | Frame Resync Criteria 0 = resync if FAS received in error three consecutive times 1 = resync if FAS or bit 2 of non-FAS is received in error three consecutive times |
| SYNCE | 1 | Sync Enable 0 = auto resync enabled 1 = auto resync disabled |
| RESYNC | 0 | Resync. When toggled from low to high, a resync is initiated. Must be cleared and set again for a subsequent resync. |

Table 8-A. Sync/Resync Criteria

| FRAME OR MULTIFRAME LEVEL | SYNC CRITERIA | RESYNC CRITERIA | ITU SPEC. |
|---------------------------|--|---|-------------------------|
| FAS | FAS present in frame N and N + 2, and FAS not present in frame N + 1 | Three consecutive incorrect FAS received; alternate (RCR1.2 = 1): if the above criteria is met or three consecutive incorrect bit 2 of non-FAS received | G.706 4.1.1 4.1.2 |
| CRC4 | Two valid MF alignment words found within 8ms | 915 or more CRC4 codewords out of 1000 received in error | G.706 4.2 and 4.3.2 |
| CAS | Valid MF alignment word found and previous time slot 16 contains code other than all zeros | Two consecutive MF alignment words received in error | G.732 5.2 |

Register Name: **TCR**
Register Description: **Transmit Control Register**
Register Address: **11 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|-----|------|
| Name | IFSS | TFPT | AEBE | TUA1 | TSiS | TSA1 | TSM | TSIO |

| NAME | BIT | FUNCTION |
|------|-----|---|
| IFSS | 7 | Internal Frame-Sync Select 0 = TSYNC normal 1 = if TSYNC is in the INPUT mode (TSIO = 0), then TSYNC is internally replaced by the recovered receive frame sync. The TSYNC pin is ignored 1 = if TSYNC is in the OUTPUT mode (TSIO = 1), then TSYNC outputs the recovered multiframe frame sync |
| TFPT | 6 | Transmit Time Slot 0 Pass Through 0 = FAS bits/Sa bits/remote alarm sourced internally from the TAF and TNAF registers 1 = FAS bits/Sa bits/remote alarm sourced from TSER |
| AEBE | 5 | Automatic E-Bit Enable 0 = E-bits not automatically set in the transmit direction 1 = E-bits automatically set in the transmit direction |
| TUA1 | 4 | Transmit Unframed All Ones 0 = transmit data normally 1 = transmit an unframed all-ones code |
| TSiS | 3 | Transmit International Bit Select 0 = sample Si bits at TSER pin 1 = source Si bits from TAF and TNAF registers (In this mode, TCR.6 must be set to 0) |
| TSA1 | 2 | Transmit Signaling All Ones 0 = normal operation 1 = force time slot 16 in every frame to all ones |
| TSM | 1 | TSYNC Mode Select 0 = frame mode (see the timing diagrams in Section 24.2) 1 = CAS and CRC4 multiframe mode (see the timing diagrams in Section 24.2) |
| TSIO | 0 | TSYNC I/O Select 0 = TSYNC is an input 1 = TSYNC is an output |

Note: See [Figure 24-9](#) for more details about how the transmit control register affects DS21Q59 operation.

Register Name: **CCR1**
 Register Description: **Common Control Register 1**
 Register Address: **12 Hex**

| | | | | | | | | |
|-------|-----|-------|------|-------|------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FLB | THDB3 | TIBE | TCRC4 | RSMS | RHDB3 | PCLMS | RCRC4 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| FLB | 7 | Framer Loopback. See Section 8.2 for details. 0 = loopback disabled 1 = loopback enabled |
| THDB3 | 6 | Transmit HDB3 Enable 0 = HDB3 disabled 1 = HDB3 enabled |
| TIBE | 5 | Transmit Insert Bit Error. A 0-to-1 transition causes a single bit error to be inserted in the transmit path. |
| TCRC4 | 4 | Transmit CRC4 Enable 0 = CRC4 disabled 1 = CRC4 enabled |
| RSMS | 3 | Receive Signaling Mode Select 0 = CAS signaling mode. Receiver searches for the CAS MF alignment signal. 1 = CCS signaling mode. Receiver does not search for the CAS MF alignment signal. |
| RHDB3 | 2 | Receive HDB3 Enable 0 = HDB3 disabled 1 = HDB3 enabled |
| PCLMS | 1 | Per-Channel Loopback Mode Select. See Section 17 for details. 0 = remote per-channel loopback 1 = local per-channel loopback |
| RCRC4 | 0 | Receive CRC4 Enable 0 = CRC4 disabled 1 = CRC4 enabled |

8.2 Framer Loopback

When CCR1.7 is set to 1, the DS21Q59 enters a framer loopback (FLB) mode ([Figure 3-1](#)). This loopback is useful in testing and debugging applications. In FLB mode, the SCT loops data from the transmitter back to the receiver. When FLB is enabled, the following occurs:

- 1) Data is transmitted as normal at TPOSO and TNEGO.
- 2) Data input through RPOSI and RNEGI is ignored.
- 3) The RCLK output is replaced with the TCLK input.

Register Name: **CCR2**
 Register Description: **Common Control Register 2**
 Register Address: **13 Hex**

| | | | | | | | | |
|-------|------|-------|------|-----|-------|--------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | ECUS | VCRFS | AAIS | ARA | RSERC | LOTCMC | RCLA | TCSS |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| ECUS | 7 | Error Counter Update Select. See Section 10 for details. 0 = update error counters once a second 1 = update error counters every 62.5ms (500 frames) |
| VCRFS | 6 | VCR Function Select. See Section 10 for details. 0 = count bipolar violations (BPVs) 1 = count code violations (CVs) |
| AAIS | 5 | Automatic AIS Generation 0 = disabled 1 = enabled |
| ARA | 4 | Automatic Remote Alarm Generation 0 = disabled 1 = enabled |
| RSERC | 3 | RSER Control 0 = allow RSER to output data as received under all conditions 1 = force RSER to 1 under loss-of-frame alignment conditions |
| LOTCMC | 2 | Loss-of-Transmit Clock Mux Control. Determines whether the transmit formatter should switch to the ever present RCLK if the TCLK should fail to transition. 0 = do not switch to RCLK if TCLK stops 1 = switch to RCLK if TCLK stops |
| RCLA | 1 | Receive Carrier Loss (RCL) Alternate Criteria 0 = RCL declared upon 255 consecutive 0s (125µs) 1 = RCL declared upon 2048 consecutive 0s (1ms) |
| TCSS | 0 | Transmit Clock Source Select. This function allows the user to internally select RCLK as the clock source for the transmit formatter. 0 = source of transmit clock is determined by CCR2.2 (LOTCMC) 1 = forces transmitter to internally switch to RCLK as source of transmit clock; signal at TCLK pin is ignored |

8.3 Automatic Alarm Generation

The device can be programmed to automatically transmit AIS or remote alarm. When automatic AIS generation is enabled (CCR2.5 = 1), the device monitors the receive framer to determine if any of the following conditions are present: loss-of-receive frame synchronization, AIS alarm (all ones) reception, or loss-of-receive carrier (or signal). If one (or more) of these conditions is present, the framer forces an AIS alarm.

When automatic RAI generation is enabled (CCR2.4 = 1), the receiver is monitored to determine if any of the following conditions are present: loss-of-receive frame synchronization, AIS alarm (all ones) reception, or loss-of-receive carrier (or signal), or if CRC4 multiframe synchronization cannot be found within 128ms of FAS synchronization (if CRC4 is enabled). If one (or more) of these conditions is present, the device transmits an RAI alarm. RAI generation conforms to ETS 300 011 specifications, and a constant remote alarm is transmitted if the DS21Q59 cannot find CRC4 multiframe synchronization within 400ms as per G.706.

Register Name: **CCR3**
 Register Description: **Common Control Register**
 Register Address: **14 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----|-------|------|------|------|------|------|
| Name | RLB | LLB | LIAIS | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| RLB | 7 | Remote Loopback. See Section 8.4 for details. 0 = loopback disabled 1 = loopback enabled |
| LLB | 6 | Local Loopback. See Section 8.5 for details. 0 = loopback disabled 1 = loopback enabled |
| LIAIS | 5 | Line Interface AIS-Generation Enable 0 = allow normal data to be transmitted at TTIP and TRING 1 = force unframed all ones to be transmitted at TTIP and TRING at the MCLK rate |
| TCM4 | 4 | Transmit Channel Monitor Bit 4. MSB of a channel decode that determines which transmit channel data appears in the TDS0M register. See Section 10 or details. |
| TCM3 | 3 | Transmit Channel Monitor Bit 3 |
| TCM2 | 2 | Transmit Channel Monitor Bit 2 |
| TCM1 | 1 | Transmit Channel Monitor Bit 1 |
| TCM0 | 0 | Transmit Channel Monitor Bit 0. LSB of the channel decode. |

8.4 Remote Loopback

When CCR4.7 is set to 1, the DS21Q59 is forced into remote loopback (RLB) mode. In this loopback, data input through the RPOSI and RNEGI pins is transmitted back to the TPOSO and TNEGO pins. Data continues to pass through the DS21Q59's receive framer as it would normally and the data from the transmit formatter is ignored ([Figure 3-1](#)).

8.5 Local Loopback

When CCR4.6 is set to 1, the DS21Q59 is forced into local loopback (LLB) mode. In this loopback, data continues to be transmitted as normal. Data being received at RTIP and RRING is replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator ([Figure 3-1](#)).

Register Name: **CCR4**
 Register Description: **Common Control Register 4**
 Register Address: **15 Hex**

| | | | | | | | | |
|-------|-------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LIRST | RESA | RESR | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| LIRST | 7 | Line Interface Reset. Setting this bit from 0 to 1 initiates an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. It must be cleared and set again for a subsequent reset. |
| RESA | 6 | Receive Elastic Store Align. Setting this bit from 0 to 1 may force the receive elastic store's write/read pointers to a minimum separation of half a frame. No action is taken if the pointer separation is already greater than or equal to half a frame. If pointer separation is less than half a frame, the command is executed and data is disrupted. This bit should be toggled after SYSCLK has been applied and is stable. It must be cleared and set again for a subsequent align. See Section 18 for details. |
| RESR | 5 | Receive Elastic Store Reset. Setting this bit from 0 to 1 forces the receive elastic store to a depth of one frame. Receive data is lost during the reset. The bit should be toggled after SYSCLK has been applied and is stable. It must be cleared and set again for a subsequent reset. See Section 18 for details. |
| RCM4 | 4 | Receive Channel Monitor Bit 4. MSB of a channel decode that determines which receive channel data appears in the RDS0M register. See Section 10 for details. |
| RCM3 | 3 | Receive Channel Monitor Bit 3 |
| RCM2 | 2 | Receive Channel Monitor Bit 2 |
| RCM1 | 1 | Receive Channel Monitor Bit 1 |
| RCM0 | 0 | Receive Channel Monitor Bit 0. LSB of the channel decode. |

Register Name: **CCR5**
 Register Description: **Common Control Register 5**
 Register Address: **16 Hex**

| | | | | | | | | |
|-------|--------|------|-------|--------|--------|--------|--------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LIUODO | CDIG | LIUSI | IRTSEL | TPRBS1 | TPRBS0 | RPRBS1 | RPRBS0 |

| NAME | BIT | FUNCTION |
|--------|-----|--|
| LIUODO | 7 | Line Interface Open-Drain Option. This control bit determines whether or not the TTIP and TRING outputs are open drain. The line driver outputs can be forced open drain to allow $6V_{PEAK}$ pulses to be generated or to allow the creation of a very low power interface. 0 = allow TTIP and TRING to operate normally 1 = force the TTIP and TRING outputs to be open drain |
| CDIG | 6 | Customer Disconnect Indication Generator. This control bit determines whether the line interface generates an unframed ...1010... pattern at TTIP and TRING instead of the normal data pattern. 0 = generate normal data at TTIP and TRING 1 = generate a ...1010... pattern at TTIP and TRING |
| LIUSI | 5 | Line Interface G.703 Synchronization Interface Enable. This control bit works with CCR7.0 to select G.703 functionality on the transmitter and receiver (Table 8-B). These bits determine whether the line receiver and transmitter should receive/transmit a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703). |
| IRTSEL | 4 | Receive Termination Select. This function applies internal parallel resistance to the normal 120Ω external termination to create a 75Ω termination. 0 = normal 120Ω external termination 1 = internally adjust receive termination to 75Ω |
| TPRBS1 | 3 | Transmit PRBS Mode Bit 1 |
| TPRBS0 | 2 | Transmit PRBS Mode Bit 0 |
| RPRBS1 | 1 | Receive PRBS Mode Bit 1 |
| RPRBS0 | 0 | Receive PRBS Mode Bit 0 |

Table 8-B. G.703 Function

| LIUSI (CCR5.5) | TG703 (CCR7.0) | FUNCTION |
|-------------------|-------------------|--|
| 0 | 0 | Transmit and receive function normally |
| 0 | 1 | Transmit G.703 signal, receiver functions normally |
| 1 | 0 | Transmit and receive G.703 signal |
| 1 | 1 | Receive G.703, transmitter functions normally |

Register Name: **CCR6**
 Register Description: **Common Control Register 6**
 Register Address: **2F Hex**

| | | | | | | | | |
|-------|------|------|------|--------|------|---|---|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | OTM1 | OTM0 | SRAS | LTC/SC | T16S | — | — | RESET |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| OTM1 | 7 | Output Test Mode 1 (Table 8-C) |
| OTM0 | 6 | Output Test Mode 0 (Table 8-C) |
| SRAS | 5 | Signaling Read Access Select. This bit controls the function of registers SA1 through SA16 when reading. 0 = reading SA1–SA16 accesses receive signaling data 1 = reading SA1–SA16 accesses transmit signaling data |
| LTC/SC | 4 | Loss-of-Transmit Clock/Signaling Change-of-State Select. This bit determines how the status register bit at SR2.2 operates. 0 = SR2.2 indicates loss-of-transmit clock 1 = SR2.2 indicates signaling data has changed states since the last multiframe |
| T16S | 3 | Time Slot 16 Select. Transmit signaling insertion enable. 0 = signaling is not inserted into the transmit path from SA1–SA16 1 = signaling is inserted into the transmit path from SA1–SA16 |
| — | 2 | Unused. Should be set = 0 for proper operation. |
| — | 1 | Unused. Should be set = 0 for proper operation. |
| RESET | 0 | Reset. A low-to-high transition of this bit resets all register bits to 0. |

Table 8-C. Output Modes

| OTM1 | OTM0 | OUTPUTS |
|------|------|----------------------|
| 0 | 0 | Normal Operation |
| 0 | 1 | Outputs in Tri-State |
| 1 | 0 | Outputs Low |
| 1 | 1 | Outputs High |

Register Name: **CCR7**
 Register Description: **Common Control Register 7**
 Register Address: **1F Hex**

| | | | | | | | | |
|-------|---|---|---|---|------|-----|---|-------|
| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name: | — | — | — | — | 136S | ALB | — | TG703 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| — | 7 | Unused. Should be set = 0 for proper operation. |
| — | 6 | Unused. Should be set = 0 for proper operation. |
| — | 5 | Unused. Should be set = 0 for proper operation. |
| — | 4 | Unused. Should be set = 0 for proper operation. |
| 136S | 3 | 1:1.36 Transformer Select 0 = 1:2 transmit transformer 1 = 1:1.36 or 1:1.6 transmit transformer (see table below for details) |
| ALB | 2 | Analog Loopback. Setting this bit internally connects TTIP and TRING to RTIP and RRING. The external signal at the RTIP and RRING pins is ignored. |
| — | 1 | Unused. Should be set = 0 for proper operation. |
| TG703 | 0 | Transmit G.703. This control bit works with CCR5.5 to select G.703 functionality on the transmitter and receiver (Table 8-B). These bits determine whether the line receiver and transmitter should receive/transmit a normal E1 signal (Section 6 of G.703) or a 2.048MHz synchronization signal (Section 10 of G.703). |

| 136S | L2 | L1 | L0 | APPLICATION | TRANSFORMER 1:1.6 | TRANSFORMER 1:1.36 |
|------|----|----|----|-------------|----------------------|-----------------------|
| 1 | 0 | 0 | 0 | 75Ω | Rt = 0Ω | N.M. |
| 1 | 0 | 0 | 1 | 120Ω | Rt = 0Ω | N.M. |
| 1 | 0 | 1 | 0 | 75Ω | Rt = 2.7Ω | Rt = 0Ω |
| 1 | 0 | 1 | 1 | 120Ω | Rt = 3.3Ω | Rt = 0Ω |
| 1 | 1 | 0 | 0 | N.M. | N.M. | N.M. |
| 1 | 1 | 0 | 1 | N.M. | N.M. | N.M. |
| 1 | 1 | 1 | 0 | N.M. | N.M. | N.M. |
| 1 | 1 | 1 | 1 | N.M. | N.M. | N.M. |

N.M. = Not meaningful

9. STATUS AND INFORMATION REGISTERS

The DS21Q59 has a set of four registers that contain information about a framer's real-time status. The registers include status register 1 (SR1), status register 2 (SR2), receive information register (RIR), and synchronizer status register (SSR).

When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers is set to 1. All the bits in the SR1, SR2, and RIR1 registers operate in a latched fashion. The SSR contents are not latched, which means that if an event or an alarm occurs and a bit is set to 1 in any of the registers, the bit remains set until the user reads that bit. The bit is cleared when it is read and is not set again until the event has occurred again (or, in the case of the RUA1, RRA, RCL, and RLOS alarms, the bit remains set if the alarm is still present).

The user always precedes a read of the SR1, SR2, and RIR registers with a write. The byte written to the register informs the framer which bits the user wishes to read and have cleared. The user writes a byte to one of these registers with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register updates with the latest information. When a 0 is written to a bit position, the read register does not update and the previous value is held. A write to the status and information registers is immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written, and this value should be written back into the same register to ensure the bit clears. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access through the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS21Q59 with higher-order software languages.

The SSR register operates differently than the other three. It is a read-only register and reports the status of the synchronizer in real time. This register is not latched and it is not necessary to precede a read of this register with a write.

The SR1 and SR2 registers have the unique ability to initiate a hardware interrupt through the $\overline{\text{INT}}$ output pin. Each of the alarms and events in SR1 and SR2 can be either masked or unmasked from the interrupt pin through interrupt mask register 1 (IMR1) and interrupt mask register 2 (IMR2).

The interrupts caused by alarms in SR1 (RUA1, RRA, RCL, and RLOS) act differently than the interrupts caused by events in SR1 and SR2 (RSA1, RDMA, RSA0, RSLIP, RMF, TMF, SEC, TAF, LOTC, and RCMF). The alarm-caused interrupts force the $\overline{\text{INT}}$ pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in [Table 9-A](#)). The $\overline{\text{INT}}$ pin is allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur, even if the alarm is still present.

The event-based interrupts force the $\overline{\text{INT}}$ pin low when the event occurs. The $\overline{\text{INT}}$ pin returns high () when the user reads the event bit that caused the interrupt to occur. Furthermore, some event-based interrupts occur continuously as long as the event is occurring (RSLIP, SEC, TMF, RMF, TAF, RAF, RCMF). Other event-based interrupts force the $\overline{\text{INT}}$ pin low only once when the event is first detected (LOTC, PRSBD, RDMA, RSA1, RSA0), that is, the PRSBD interrupt fires once when the receiver detects the PRBS pattern. If the receiver continues to receive the PRBS pattern, no more interrupts are fired. If the receiver then detects that PRBS is no longer being sent, it resets and, when it receives the PRBS pattern again, another interrupt is fired.

9.1 Interrupt Handling

The host can quickly determine which status registers in the four ports are causing an interrupt by reading one of the unused addresses such as 0Ch, 0Dh, or 0Eh in any port.

| | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SR2P4 | SR1P4 | SR2P3 | SR1P3 | SR2P2 | SR1P2 | SR2P1 | SR1P1 |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| SR2P4 | 7 | Status Register 2, Port 4. A 1 in this bit position indicates that status register 2 in port 4 is asserting an interrupt. |
| SR1P4 | 6 | Status Register 1, Port 4. A 1 in this bit position indicates that status register 1 in port 4 is asserting an interrupt. |
| SR2P3 | 5 | Status Register 2, Port 3. A 1 in this bit position indicates that status register 2 in port 3 is asserting an interrupt. |
| SR1P3 | 4 | Status Register 1, Port 3. A 1 in this bit position indicates that status register 1 in port 3 is asserting an interrupt. |
| SR2P2 | 3 | Status Register 2, Port 2. A 1 in this bit position indicates that status register 2 in port 2 is asserting an interrupt. |
| SR1P2 | 2 | Status Register 1, Port 2. A 1 in this bit position indicates that status register 1 in port 2 is asserting an interrupt. |
| SR2P1 | 1 | Status Register 2, Port 1. A 1 in this bit position indicates that status register 2 in port 1 is asserting an interrupt. |
| SR1P1 | 0 | Status Register 1, Port 1. A 1 in this bit position indicates that status register 1 in port 1 is asserting an interrupt. |

Register Name: **RIR**
 Register Description: **Receive Information Register**
 Register Address: **08 Hex**

| | | | | | | | | |
|-------|------|------|------|------|------|-------|-------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RGM1 | RGM0 | JALT | RESF | RESE | CRCRC | FASRC | CASRC |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| RGM1 | 7 | Receive Gain Monitor Bit 1. See table below for level indication. |
| RGM0 | 6 | Receive Gain Monitor Bit 0. See table below for level indication. |
| JALT | 5 | Jitter Attenuator Limit Trip. Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation. |
| RESF | 4 | Receive Elastic Store Full. Set when the receive elastic store buffer fills and a frame is deleted. |
| RESE | 3 | Receive Elastic Store Empty. Set when the receive elastic store buffer empties and a frame is repeated. |
| CRCRC | 2 | CRC Resync Criteria Met. Set when 915/1000 codewords are received in error. |
| FASRC | 1 | FAS Resync Criteria Met. Set when three consecutive FAS words are received in error. |
| CASRC | 0 | CAS Resync Criteria Met. Set when two consecutive CAS MF alignment words are received in error. |

Level Indication

| RGM1 | RGM0 | LEVEL (dB) |
|------|------|------------|
| 0 | 0 | 0 to 10 |
| 0 | 1 | 10 to 20 |
| 1 | 0 | 20 to 30 |
| 1 | 1 | >30 |

Register Name: **SSR**
 Register Description: **Synchronizer Status Register**
 Register Address: **09 Hex**

| | | | | | | | | |
|-------|------|------|------|------|------|-------|-------|--------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | CSC5 | CSC4 | CSC3 | CSC2 | CSC0 | FASSA | CASSA | CRC4SA |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| CSC5 | 7 | CRC4 Sync Counter Bit 5. MSB of the 6-bit counter. |
| CSC4 | 6 | CRC4 Sync Counter Bit 4 |
| CSC3 | 5 | CRC4 Sync Counter Bit 3 |
| CSC2 | 4 | CRC4 Sync Counter Bit 2 |
| CSC0 | 3 | CRC4 Sync Counter Bit 0. LSB of the 6-bit counter. Counter bit 1 is not accessible. |
| FASSA | 2 | FAS Sync Active. Set while the synchronizer is searching for alignment at the FAS level. |
| CASSA | 1 | CAS MF Sync Active. Set while the synchronizer is searching for the CAS MF alignment word. |
| CRC4SA | 0 | CRC4 MF Sync Active. Set while the synchronizer is searching for the CRC4 MF alignment word. |

9.2 CRC4 Sync Counter

The CRC4 sync counter increments each time the 8ms CRC4 multiframe search times out. The counter is cleared when the framer has successfully obtained synchronization at the CRC4 level. The counter can also be cleared by disabling the CRC4 mode (CCR1.0 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC4 level. ITU G.706 suggests that if synchronization at the CRC4 level cannot be obtained within 400ms, the search should be abandoned and proper action taken. The CRC4 sync counter rolls over.

Table 9-A. Alarm Criteria

| ALARM | SET CRITERIA | CLEAR CRITERIA | ITU SPEC |
|---|--|--|------------------|
| RSA1 (Receive Signaling All Ones) | Over 16 consecutive frames (one full MF) time slot 16 contains less than three zeros | Over 16 consecutive frames (one full MF) time slot 16 contains three or more zeros | G.732 4.2 |
| RSA0 (Receive Signaling All Zeros) | Over 16 consecutive frames (one full MF) time slot 16 contains all zeros | Over 16 consecutive frames (one full MF) time slot 16 contains at least a single one | G.732 5.2 |
| RDMA (Receive Distant Multiframe Alarm) | Bit 6 in time slot 16 of frame 0 set to one for two consecutive MF | Bit 6 in time slot 16 of frame 0 set to zero for two consecutive MF | O.162 2.1.5 |
| RUA1 (Receive Unframed All Ones) | Fewer than three zeros in two frames (512 bits) | More than two zeros in two frames (512 bits) | O.162 1.6.1.2 |
| RRA (Receive Remote Alarm) | Bit 3 of nonalign frame set to one for three consecutive occasions | Bit 3 of nonalign frame set to zero for three consecutive occasions | O.162 2.1.4 |
| RCL (Receive Carrier Loss) | 255 (or 2048) consecutive zeros received | In 255-bit times at least 32 ones are received | G.775/ G.962 |

Register Name: **SR1**
 Register Description: **Status Register 1**
 Register Address: **0A Hex**

| | | | | | | | | |
|-------|------|------|------|-------|------|-----|-----|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RSA1 | RDMA | RSA0 | RSLIP | RUA1 | RRA | RCL | RLOS |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| RSA1 | 7 | Receive Signaling All Ones. Set when the contents of time slot 16 contains fewer than three zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode. Both RSA1 and RSA0 are set if a change in signaling is detected. |
| RDMA | 6 | Receive Distant MF Alarm. Set when bit 6 of time slot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode. |
| RSA0 | 5 | Receive Signaling All Zeros. Set when over a full MF, time slot 16 contains all zeros. Both RSA1 and RSA0 are set if a change in signaling is detected. |
| RSLIP | 4 | Receive Elastic Store Slip. Set when the elastic store has either repeated or deleted a frame of data. |
| RUA1 | 3 | Receive Unframed All Ones. Set when an unframed all-ones code is received at RPOSI and RNEGI. |
| RRA | 2 | Receive Remote Alarm. Set when a remote alarm is received at RPOSI and RNEGI. |
| RCL | 1 | Receive Carrier Loss. Set when 255 (or 2048 if CCR2.1 = 1) consecutive zeros have been detected at RTIP and RRING. (Note: A receiver carrier loss based on data received at RPOSI and RNEGI is available in the HSR register.) |
| RLOS | 0 | Receive Loss of Sync. Set when the device is not synchronized to the receive E1 stream. |

Register Name: **IMR1**
 Register Description: **Interrupt Mask Register 1**
 Register Address: **18 Hex**

| | | | | | | | | |
|-------|------|------|------|-------|------|-----|-----|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RSA1 | RDMA | RSA0 | RSLIP | RUA1 | RRA | RCL | RLOS |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| RSA1 | 7 | Receive Signaling All Ones 0 = interrupt masked 1 = interrupt enabled |
| RDMA | 6 | Receive Distant MF Alarm 0 = interrupt masked 1 = interrupt enabled |
| RSA0 | 5 | Receive Signaling All Zeros 0 = interrupt masked 1 = interrupt enabled |
| RSLIP | 4 | Receive Elastic Store Slip Occurrence 0 = interrupt masked 1 = interrupt enabled |
| RUA1 | 3 | Receive Unframed All Ones 0 = interrupt masked 1 = interrupt enabled |
| RRA | 2 | Receive Remote Alarm 0 = interrupt masked 1 = interrupt enabled |
| RCL | 1 | Receive Carrier Loss 0 = interrupt masked 1 = interrupt enabled |
| RLOS | 0 | Receive Loss of Sync 0 = interrupt masked 1 = interrupt enabled |

Register Name: **SR2**
 Register Description: **Status Register 2**
 Register Address: **0B Hex**

| | | | | | | | | |
|-------|-----|-----|-----|-----|-----|------|------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RMF | RAF | TMF | SEC | TAF | LOTC | RCMF | PRBSD |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| RMF | 7 | Receive CAS Multiframe. Set every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. |
| RAF | 6 | Receive Align Frame. Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers. |
| TMF | 5 | Transmit Multiframe. Set every 2ms (regardless if CRC4 is enabled) on transmit multiframe boundaries. |
| SEC | 4 | One-Second Timer. Set on increments of one second based on RCLK. If CCR2.7 = 1, this bit is set every 62.5ms instead of once a second. |
| TAF | 3 | Transmit Align Frame. Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated. |
| LOTC | 2 | Loss-of-Transmit Clock. Set when the TCLK pin has not transitioned for one channel time (or 3.9ms). |
| RCMF | 1 | Receive CRC4 Multiframe. Set on CRC4 multiframe boundaries; continues to be set every 2ms on an arbitrary boundary if CRC4 is disabled. |
| PRBSD | 0 | Pseudorandom Bit-Sequence Detect. When receive PRBS is enabled, this bit is set when the $2^{15} - 1$ PRBS pattern is detected at RPOS and RNEG. The PRBS pattern can be framed, unframed, or in a specific time slot. |

Register Name: **IMR2**
 Register Description: **Interrupt Mask Register 2**
 Register Address: **19 Hex**

| | | | | | | | | |
|-------|-----|-----|-----|-----|-----|------|------|-------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RMF | RAF | TMF | SEC | TAF | LOTC | RCMF | PRBSD |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| RMF | 7 | Receive CAS Multiframe 0 = interrupt masked 1 = interrupt enabled |
| RAF | 6 | Receive Align Frame 0 = interrupt masked 1 = interrupt enabled |
| TMF | 5 | Transmit Multiframe 0 = interrupt masked 1 = interrupt enabled |
| SEC | 4 | One-Second Timer 0 = interrupt masked 1 = interrupt enabled |
| TAF | 3 | Transmit Align Frame 0 = interrupt masked 1 = interrupt enabled |
| LOTC | 2 | Loss-of-Transmit Clock 0 = interrupt masked 1 = interrupt enabled |
| RCMF | 1 | Receive CRC4 Multiframe 0 = interrupt masked 1 = interrupt enabled |
| PRBSD | 0 | Pseudorandom Bit-Sequence Detect 0 = interrupt masked 1 = interrupt enabled |

10. ERROR COUNT REGISTERS

Each DS21Q59 transceiver contains a set of four counters that record bipolar (BPVs) or code violations (CVs), errors in the CRC4 SMF codewords, E bits as reported by the far end, and word errors in the FAS. The E-bit counter is reconfigured for counting errors in the PRBS pattern if receive PRBS is enabled. Each of these four counters is automatically updated on either one-second boundaries (CCR2.70 = 0) or every 62.5ms (CCR2.7 = 1) as determined by the timer in status register 2 (SR2.4). Hence, these registers contain performance data from either the previous second or the previous 62.5ms. The user can use the interrupt from the one-second timer to determine when to read these registers. The user has a full second (or 62.5ms) to read the counters before the data is lost. The counters saturate at their respective maximum counts and do not roll over.

10.1 BPV or CV Counter

Violation count register 1 (VCR1) is the most significant word and VCR2 is the least significant word of a 16-bit counter that records either BPVs or CVs. If CCR2.6 = 0, the VCR counts BPVs. BPVs are defined as consecutive marks of the same polarity. In this mode, if the HDB3 mode is set for the receiver through CCR1.2, then HDB3 codewords are not counted as BPVs. If CCR2.6 = 1, the VCR counts CVs as defined in ITU O.161. CVs are defined as consecutive BPVs of the same polarity. In most applications, the framer should be programmed to count BPVs when receiving AMI code and to count CVs when receiving HDB3 code. This counter increments at all times and is not disabled by loss-of-sync conditions. The counter saturates at 65,535 and does not roll over. The bit-error rate on an E1 line would have to be greater than 10^{-2} before the VCR would saturate.

Register Name: **VCR1, VCR2**
 Register Description: **Bipolar Violation Count Registers**
 Register Address: **00 Hex, 01 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----|-----|-----|-----|-----|----|----|
| Name | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 |
| | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |

| NAME | BIT | FUNCTION |
|------|--------|---|
| V15 | VCR1.7 | MSB of the 16-bit code violation count. |
| V0 | VCR2.0 | LSB of the 16-bit code violation count. |

10.2 CRC4 Error Counter

CRC4 count register 1 (CRCCR1) is the most significant word and CRCCR2 is the least significant word of a 16-bit counter that records word errors in the cyclic redundancy check 4 (CRC4). Since the maximum CRC4 count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it continues to count if loss-of-multiframe sync occurs at the CAS level. CRCCR1 and CRCCR2 have an alternate function.

Register Name: **CRCCR1, CRCCR2**
 Register Description: **CRC4 Count Registers**
 Register Address: **02 Hex, 03 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|------|------|
| Name | CRC15 | CRC14 | CRC13 | CRC12 | CRC11 | CRC10 | CRC9 | CRC8 |
| | CRC7 | CRC6 | CRC5 | CRC4 | CRC/3 | CRC2 | CRC1 | CRC0 |

| NAME | BIT | FUNCTION |
|-------|----------|-------------------------------------|
| CRC15 | CRCCR1.7 | MSB of the 16-bit CRC4 error count. |
| CRC0 | CRCCR2.0 | LSB of the 16-bit CRC4 error count. |

10.3 E-Bit/PRBS Bit-Error Counter

E-bit count register 1 (EBCR1) is the most significant word and EBCR2 is the least significant word of a 16-bit counter that records far-end block errors (FEBE) as reported in the first bit of frames 13 and 15 on E1 lines running with CRC4 multiframe. These error count registers increment once each time the received E-bit is set to 0. Since the maximum E-bit count in a one-second period is 1000, this counter cannot saturate. The counter is disabled during loss of sync at either the FAS or CRC4 level; it continues to count if loss-of-multiframe sync occurs at the CAS level.

Alternately, this counter counts bit errors in the received PRBS pattern when the receive PRBS function is enabled. In this mode, the counter is active when the receive PRBS detector can synchronize to the PRBS pattern. This pattern can be framed, unframed, or in any time slot. See Section 13 for more details.

Register Name: **EBCR1, EBCR2**
 Register Description: **E-Bit Count Registers**
 Register Address: **04 Hex, 05 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|-----|-----|
| Name | EB15 | EB14 | EB13 | EB12 | EB11 | EB10 | EB9 | EB8 |
| | EB7 | EB6 | EB5 | EB4 | EB3 | EB2 | EB1 | EB0 |

| NAME | BIT | FUNCTION |
|------|---------|--------------------------------------|
| EB15 | EBCR1.7 | MSB of the 16-bit E-bit error count. |
| EB0 | EBCR2.0 | LSB of the 16-bit E-bit error count. |

10.4 FAS Error Counter

FAS count register 1 (FASCR1) is the most significant word and FASCR2 is the least significant word of a 16-bit counter that records word errors in the FAS in time slot 0. This counter is disabled when RLOS is high. FAS errors are not counted when the framer is searching for FAS alignment and/or synchronization at either the CAS or CRC4 multiframe level. Since the maximum FAS word error count in a one-second period is 4000, this counter cannot saturate.

Register Name: **FASCR1, FASCR2**
 Register Description: **FAS Error Count Registers**
 Register Address: **06 Hex, 07 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|------|------|
| Name | FAS15 | FAS14 | FAS13 | FAS12 | FAS11 | FAS10 | FAS9 | FAS8 |
| | FAS7 | FAS6 | FAS5 | FAS4 | FAS3 | FAS2 | FAS1 | FAS0 |

| NAME | BIT | FUNCTION |
|-------|----------|------------------------------------|
| FAS15 | FASCR1.7 | MSB of the 16-bit FAS error count. |
| FAS0 | FASCR2.0 | LSB of the 16-bit FAS error count. |

11. SIGNALING OPERATION

Registers SA1 and SA16 are used to access the transmit and receive signaling function. Normally, reading these registers accesses the receive signaling data and writing these registers sources signaling data for the transmitter. The user can read what was written to the transmit signaling buffer by setting CCR6.5 = 1, then reading SA1–SA16. In most applications, however, CCR6.5 should be set = 0.

11.1 Receive Signaling

Signaling data is sampled from time slot 16 in the receive data stream and copied into the receive signaling buffers. The host can access the signaling data by reading SA1 through SA16. The signaling information in these registers is always updated on multiframe boundaries. The SR2.7 bit in status register 2 can be used to alert the host that new signaling data is present in the receive signaling buffers. The host has 2ms to read the signaling buffers before they are updated.

11.2 Transmit Signaling

Insertion of signaling data from the transmit signaling buffers is enabled by setting CCR6.3 = 1. Signaling data is loaded into the transmit signaling buffers by writing the signaling data to SA1–SA16. On multiframe boundaries, the contents of the transmit signaling buffer is loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can use the transmit multiframe interrupt in status register 2 (SR2.5) to know when to update the signaling bits. The host has 2ms to update the signaling data. The user only needs to update the signaling data that has changed since the last update.

11.3 CAS Operation

For CAS mode, the user must provide the CAS alignment pattern (four 0s in the upper nibble of TS16). Typically this is done by setting the upper four bits of SA1 = 0. The lower four bits are alarm bits. The user only needs to update the appropriate channel associated signaling data in SA2–SA16 on multiframe boundaries.

Register Name: **SA1 to SA16**
 Register Description: **Signaling Registers**
 Register Address: **30h to 3Fh**

| (MSB) | | | | (LSB) | | | | |
|--------|--------|--------|--------|--------|--------|--------|--------|------|
| 0 | 0 | 0 | 0 | X | Y | X | X | |
| CH1-A | CH1-B | CH1-C | CH1-D | CH16-A | CH16-B | CH16-C | CH16-D | SA1 |
| CH2-A | CH2-B | CH2-C | CH2-D | CH17-A | CH17-B | CH17-C | CH17-D | SA2 |
| CH3-A | CH3-B | CH3-C | CH3-D | CH18-A | CH18-B | CH18-C | CH18-D | SA3 |
| CH4-A | CH4-B | CH4-C | CH4-D | CH19-A | CH19-B | CH19-C | CH19-D | SA4 |
| CH5-A | CH5-B | CH5-C | CH5-D | CH20-A | CH20-B | CH20-C | CH20-D | SA5 |
| CH6-A | CH6-B | CH6-C | CH6-D | CH21-A | CH21-B | CH21-C | CH21-D | SA6 |
| CH7-A | CH7-B | CH7-C | CH7-D | CH22-A | CH22-B | CH22-C | CH22-D | SA7 |
| CH8-A | CH8-B | CH8-C | CH8-D | CH23-A | CH23-B | CH23-C | CH23-D | SA8 |
| CH9-A | CH9-B | CH9-C | CH9-D | CH24-A | CH24-B | CH24-C | CH24-D | SA9 |
| CH10-A | CH10-B | CH10-C | CH10-D | CH25-A | CH25-B | CH25-C | CH25-D | SA10 |
| CH11-A | CH11-B | CH11-C | CH11-D | CH26-A | CH26-B | CH26-C | CH26-D | SA11 |
| CH12-A | CH12-B | CH12-C | CH12-D | CH27-A | CH27-B | CH27-C | CH27-D | SA12 |
| CH13-A | CH13-B | CH13-C | CH13-D | CH28-A | CH28-B | CH28-C | CH28-D | SA13 |
| CH14-A | CH14-B | CH14-C | CH14-D | CH29-A | CH29-B | CH29-C | CH29-D | SA14 |
| CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | SA15 |
| CH15-A | CH15-B | CH15-C | CH15-D | CH30-A | CH30-B | CH30-C | CH30-D | SA16 |

12. DS0 MONITORING FUNCTION

Each DS21Q59 framer can monitor one DS0 (64kbps) channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction, the user determines which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR3 register. In the receive direction, the RCM0 to RCM4 bits in the CCR4 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits appear in the transmit DS0 monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits appear in the receive DS0 (RDS0M) register. The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate E1 channel. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into CCR4 and CCR5:

```
TCM4 = 0    RCM4 = 0
TCM3 = 0    RCM3 = 1
TCM2 = 1    RCM2 = 1
TCM1 = 0    RCM1 = 1
TCM0 = 1    RCM0 = 0
```

Register Name: **CCR3** (Repeated here from Section 6 for convenience.)
 Register Description: **Common Control Register 3**
 Register Address: **14 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|-----|-------|------|------|------|------|------|
| Name | RLB | LLB | LIAIS | TCM4 | TCM3 | TCM2 | TCM1 | TCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| RLB | 7 | Remote Loopback |
| LLB | 6 | Local Loopback |
| LIAIS | 5 | Line Interface AIS Generation Enable |
| TCM4 | 4 | Transmit Channel Monitor Bit 4. MSB of a channel decode that determines which transmit channel data appears in the TDS0M register. See Section 10 or details. |
| TCM3 | 3 | Transmit Channel Monitor Bit 3 |
| TCM2 | 2 | Transmit Channel Monitor Bit 2 |
| TCM1 | 1 | Transmit Channel Monitor Bit 1 |
| TCM0 | 0 | Transmit Channel Monitor Bit 0. LSB of the channel decode. |

Register Name: **TDS0M**
 Register Description: **Transmit DS0 Monitor Register**
 Register Address: **22 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|----|----|----|----|----|----|----|----|
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |

| NAME | BIT | FUNCTION |
|------|-----|--|
| B1 | 7 | Transmit DS0 Channel Bit 1. MSB of the DS0 channel (first bit to be transmitted). |
| B2 | 6 | Transmit DS0 Channel Bit 2 |
| B3 | 5 | Transmit DS0 Channel Bit 3 |
| B4 | 4 | Transmit DS0 Channel Bit 4 |
| B5 | 3 | Transmit DS0 Channel Bit 5 |
| B6 | 2 | Transmit DS0 Channel Bit 6 |
| B7 | 1 | Transmit DS0 Channel Bit 7 |
| B8 | 0 | Transmit DS0 Channel Bit 8. LSB of the DS0 channel (last bit to be transmitted). |

Register Name: **CCR4** (Repeated here from Section 6 for convenience.)
 Register Description: **Common Control Register 4**
 Register Address: **15 Hex**

| | | | | | | | | |
|-------|-------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LIRST | RESA | RESR | RCM4 | RCM3 | RCM2 | RCM1 | RCM0 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| LIRST | 7 | Line Interface Reset |
| RESA | 6 | Receive Elastic Store Align |
| RESR | 5 | Receive Elastic Store Reset |
| RCM4 | 4 | Receive Channel Monitor Bit 4. MSB of a channel decode that determines which receive channel data appears in the RDS0M register. See Section 10 for details. |
| RCM3 | 3 | Receive Channel Monitor Bit 3 |
| RCM2 | 2 | Receive Channel Monitor Bit 2 |
| RCM1 | 1 | Receive Channel Monitor Bit 1 |
| RCM0 | 0 | Receive Channel Monitor Bit 0. LSB of the channel decode. |

Register Name: **RDS0M**
 Register Description: **Receive DS0 Monitor Register**
 Register Address: **2A Hex**

| | | | | | | | | |
|-------|----|----|----|----|----|----|----|----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |

| NAME | BIT | FUNCTION |
|------|-----|--|
| B1 | 7 | Receive DS0 Channel Bit 1. MSB of the DS0 channel (first bit received). |
| B2 | 6 | Receive DS0 Channel Bit 2 |
| B3 | 5 | Receive DS0 Channel Bit 3 |
| B4 | 4 | Receive DS0 Channel Bit 4 |
| B5 | 3 | Receive DS0 Channel Bit 5 |
| B6 | 2 | Receive DS0 Channel Bit 6 |
| B7 | 1 | Receive DS0 Channel Bit 7 |
| B8 | 0 | Receive DS0 Channel Bit 8. LSB of the DS0 channel (last bit received). |

13. PRBS GENERATION AND DETECTION

The DS21Q59 can transmit and receive the $2^{15} - 1$ PRBS pattern. This PRBS pattern complies with ITU-T O.151 specifications. The PRBS pattern can be unframed (in all 256 bits of the frame), framed (in all time slots except TS0), or in any single time slot. Register CCR5 contains the control bits for configuring the transmit and receives PRBS functions. See [Table 13-A](#) and [Table 13-B](#) for selecting the transmit and receive modes of operation. In transmit and receive mode 1 operation, the transmit- and receive-channel monitor-select bits of registers CCR3 and CCR4 have an alternate use. When this mode is selected, these bits determine which time slot transmits and/or receives the PRBS pattern.

SR2.0 indicates when the receiver has synchronized to the PRBS pattern. The PRBS synchronizer remains in sync until it experiences six or more bit errors within a 64-bit span. Choosing any receive mode other than NORMAL causes the 16-bit E-bit error counter—EBCR1 and EBCR2—to be reconfigured for counting PRBS errors.

User-definable outputs OUTA or OUTB can be configured to output a pulse for every bit error received. See Section 20 and [Table 20-A](#) for details. This signal can be used with external circuitry to keep track of bit-error rates during PRBS testing. Once synchronized, any bit errors received cause a positive-going pulse, synchronous with RCLK.

Table 13-A. Transmit PRBS Mode Select

| TPRBS1 (CCR5.3) | TPBRS0 (CCR5.2) | MODE |
|--------------------|--------------------|---|
| 0 | 0 | Mode 0: Normal (PRBS disabled) |
| 0 | 1 | Mode 1: PRBS in TSx. PRBS pattern is transmitted in a single time slot (TS). In this mode, the transmit-channel monitor-select bits in register CCR3 are used to select a time slot in which to transmit the PRBS pattern. |
| 1 | 0 | Mode 2: PRBS in all but TS0. PRBS pattern is transmitted in time slots 1 through 31. |
| 1 | 1 | Mode 3: PRBS unframed. PRBS pattern is transmitted in all time slots. |

Table 13-B. Receive PRBS Mode Select

| RPRBS1 (CCR5.1) | RPBRS0 (CCR5.0) | MODE |
|--------------------|--------------------|--|
| 0 | 0 | Mode 0: Normal (PRBS disabled) |
| 0 | 1 | Mode 1: PRBS in TSx. PRBS pattern is received in a single time slot (TS). In this mode, the receive-channel monitor-select bits in register CCR4 are used to select a time slot in which to receive the PRBS pattern. |
| 1 | 0 | Mode 2: PRBS in all but TS0. PRBS pattern is received in time slots 1 through 31. |
| 1 | 1 | Mode 3: PRBS unframed. PRBS pattern is received in all time slots. |

14. SYSTEM CLOCK INTERFACE

A single system clock interface (SCI) is common to all four DS21Q59 transceivers. The SCI is designed to allow any one of the four receivers to act as the master reference clock for the system. When multiple DS21Q59s are used to build an N port system, the SCI allows any one of the N ports to be the master. The selected reference is then distributed to the other DS21Q59s through the REFCLK pin. The REFCLK pin acts as an output on the DS21Q59, which has been selected to provide the reference clock from one of its four receivers. On DS21Q59s not selected to source the reference clock, this pin becomes an input by writing 0s to the SCSx bits. The reference clock is also passed to the clock synthesizer PLL to generate a 2.048MHz, 4.096MHz, 8.192MHz, or 16.384MHz clock. This clock can then be used with the IBO function to merge up to eight E1 lines onto a single high-speed PCM bus. In the event that the master E1 port fails (enters a receive carrier loss condition), that port automatically switches to the clock present on the MCLK pin. Therefore, MCLK acts as the backup source of master clock. The host can then find and select a functioning E1 port as the master. Because the selected port's clock is passed to the other DS21Q59s in a multiple device configuration, one DS21Q59's synthesizer can always be the source of the high-speed clock. This allows smooth transitions when clock-source switching occurs. The SCI control register exists in Transceiver 1 only (TS0, TS1 = 0).

Register Name: **SCICR**
 Register Description: **System Clock Interface Control Register**
 (Note: This register is valid only for Transceiver 1 (TS0 = 0, TS1 = 0).)
 Register Address: **1D Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|------|-----|------|------|------|------|------|
| Name | AJACKE | BUCS | SOE | CSS1 | CSS0 | SCS2 | SCS1 | SCS0 |

| NAME | BIT | FUNCTION |
|--------|-----|--|
| AJACKE | 7 | AJACK Enable. This bit enables the alternate jitter attenuator. |
| BUCS | 6 | Backup Clock Select. Selects which clock source to switch to automatically during a loss-of-transmit clock event. 0 = during an LOTC event switch to MCLK 1 = during an LOTC event switch to system reference clock |
| SOE | 5 | Synthesizer Output Enable 0 = 2/4/8/16MCK pin in high-Z mode 1 = 2/4/8/16MCK pin active |
| CSS1 | 4 | Clock Synthesizer Select Bit 1 (Table 14-A) |
| CSS0 | 3 | Clock Synthesizer Select Bit 0 (Table 14-A) |
| SCS2 | 2 | System Clock Select Bit 2 (Table 14-B) |
| SCS1 | 1 | System Clock Select Bit 1 (Table 14-B) |
| SCS0 | 0 | System Clock Select Bit 0 (Table 14-B) |

Table 14-A. Synthesizer Output Select

| CSS1 | CSS0 | SYNTHESIZER OUTPUT FREQUENCY (MHz) |
|------|------|------------------------------------|
| 0 | 0 | 2.048 |
| 0 | 1 | 4.096 |
| 1 | 0 | 8.192 |
| 1 | 1 | 16.384 |

Table 14-B. System Clock Selection

| SCS2 | SCS1 | SCS0 | PORT SELECTED AS MASTER |
|------|------|------|---|
| 0 | 0 | 0 | None (Master Port can be derived from another DS21Q59 in the system.) |
| 0 | 0 | 1 | Transceiver 1 |
| 0 | 1 | 0 | Transceiver 2 |
| 0 | 1 | 1 | Transceiver 3 |
| 1 | 0 | 0 | Transceiver 4 |
| 1 | 0 | 1 | Reserved for future use. |
| 1 | 1 | 0 | Reserved for future use. |
| 1 | 1 | 1 | Reserved for future use. |

15. TRANSMIT CLOCK SOURCE

Depending on the DS21Q59's operating mode, the transmit clock can be derived from different sources. In a basic configuration, where the IBO function is disabled, the transmit clock is normally sourced from the TCLK pin. In this mode, a 2.048MHz clock with ± 50 ppm accuracy is applied to the TCLK pin. If the signal at TCLK is lost, the DS21Q59 automatically switches to either the system reference clock present on the REFCLK pin or to the recovered clock off the same port, depending on which source the host assigned as the backup clock. At the same time the host can be notified of the loss-of-transmit clock through an interrupt. The host can at any time force a switchover to one of the two backup clock sources regardless of the state of the TCLK pin.

When the IBO function is enabled, the transmit clock must be synchronous to the system clock since slips are not allowed in the transmit direction. In this mode, the TCLK pin is ignored, and a transmit clock is automatically provided by the IBO circuit by dividing the clock present on the SYSCLK pin by 2, 4, or 8. In this configuration, if the signal present on the SYSCLK pin is lost, the DS21Q59 automatically switches to either the system reference clock or to the recovered clock off the same port, depending on which source the host assigned as the backup clock. The host can at any time force a switchover to one of the two backup clock sources regardless of the state of the SYSCLK pin.

16. IDLE CODE INSERTION

The transmit idle registers (TIR1/2/3/4) determine which of the 32 E1 channels should be overwritten with the code placed in the transmit idle definition register (TIDR). This allows the same 8-bit code to be placed into any of the 32 E1 channels. Each of the bit positions in the transmit idle registers represents a DS0 channel in the outgoing frame. When these bits are set to 1, the corresponding channel transmits the idle code contained in the TIDR.

Register Name: **TIR1, TIR2, TIR3, TIR4**
 Register Description: **Transmit Idle Registers**
 Register Address: **24 Hex, 25 Hex, 26 Hex, 27 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|------|------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

| NAME | BIT | FUNCTION |
|-------------|---------------|---|
| CH1 to CH32 | TIR1.0 to 4.7 | Transmit Idle Code-Insertion Control Bits 0 = do not insert the idle code in the TIDR into this channel 1 = insert the idle code in the TIDR into this channel |

Register Name: **TIDR**
 Register Description: **Transmit Idle Definition Register**
 Register Address: **23 Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Name | TIDR7 | TIDR6 | TIDR5 | TIDR4 | TIDR3 | TIDR2 | TIDR1 | TIDR0 |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| TIDR7 | 7 | MSB of the Idle Code (This bit is transmitted first.) |
| TIDR6 | 6 | — |
| TIDR5 | 5 | — |
| TIDR4 | 4 | — |
| TIDR3 | 3 | — |
| TIDR2 | 2 | — |
| TIDR1 | 1 | — |
| TIDR0 | 0 | LSB of the Idle Code (This bit is transmitted last.) |

17. PER-CHANNEL LOOPBACK

The DS21Q59 has per-channel loopback capability that can operate in one of two modes: remote per-channel loopback or local per-channel loopback. PCLB1/2/3/4 are used for both modes to determine which channels are looped back. In remote per-channel loopback mode, PCLB1/2/3/4 determine which channels (if any) in the transmit direction should be replaced with the data from the receiver or, in other words, off the E1 line. In local per-channel loopback mode, PCLB1/2/3/4 determine which channels (if any) in the receive direction should be replaced with the data from the transmit. If either mode is enabled, transmit and receive clocks and frame syncs must be synchronized. There are no restrictions on which channels can be looped back or on how many channels can be looped back.

Register Name: **PCLB1, PCLB2, PCLB3, PCLB4**
 Register Description: **Per-Channel Loopback Registers**
 Register Address: **2B Hex, 2C Hex, 2D Hex, 2E Hex**

| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|------|------|
| Name | CH8 | CH7 | CH6 | CH5 | CH4 | CH3 | CH2 | CH1 |
| | CH16 | CH15 | CH14 | CH13 | CH12 | CH11 | CH10 | CH9 |
| | CH24 | CH23 | CH22 | CH21 | CH20 | CH19 | CH18 | CH17 |
| | CH32 | CH31 | CH30 | CH29 | CH28 | CH27 | CH26 | CH25 |

| NAME | BIT | FUNCTION |
|-------------|----------------|---|
| CH1 to CH32 | PCLB1.0 to 4.7 | Per-Channel Loopback Control Bits 0 = do not loopback this channel 1 = loopback this channel |

18. ELASTIC STORE OPERATION

The DS21Q59 contains a two-frame (512 bits) elastic store for the receive direction. The elastic store is used to absorb the differences in frequency and phase between the E1 data stream and an asynchronous (i.e., not frequency locked) backplane clock that can be 2.048MHz for normal operation or 4.096MHz, 8.192MHz, or 16.384MHz when using the IBO function. The elastic store contains full controlled slip capability.

If the receive elastic store is enabled (RCR.4 = 1), the user must provide a 2.048MHz clock to the SYSCLK pin. If the IBO function is enabled, a 4.096MHz, 8.192MHz, or 16.384MHz clock must be provided at the SYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR.5 = 1) or having the RSYNC pin provide a pulse on frame/multiframe boundaries (RCR.5 = 0). If the user wishes to obtain pulses at the frame boundary, RCR1.6 must be set to 0; if the user wishes to have pulses occur at the multiframe boundary, RCR1.6 must be set to 1. If the elastic store is enabled, either CAS (RCR.7 = 0) or CRC4 (RCR.7 = 1) multiframe boundaries are indicated through the RSYNC output. See Section [24](#) for timing details. If the 512-bit elastic buffer either fills or empties, a controlled slip occurs. If the buffer empties, a full frame of data (256 bits) is repeated at RSER, and the SR1.4 and RIR.3 bits are set to 1. If the buffer fills, a full frame of data is deleted, and the SR1.4 and RIR.4 bits are set to 1.

19. ADDITIONAL (Sa) AND INTERNATIONAL (Si) BIT OPERATION

On the receiver, the RAF and RNAF registers always report the data as it is received in the additional (Sa) and international (Si) bit locations. The RAF and RNAF registers are updated with the setting of the receive align frame bit in status register 2 (SR2.6). The host can use the SR2.6 bit to know when to read the RAF and RNAF registers. It has 250 μ s to retrieve the data before it is lost.

On the transmitter, data is sampled from the TAF and TNAF registers with the setting of the transmit align frame bit in status register 2 (SR2.3). The host can use the SR2.3 bit to know when to update the TAF and TNAF registers. It has 250 μ s to update the data or else the old data is retransmitted. Data in the Si bit position is overwritten if either the framer is programmed (1) to source the Si bits from the TSER pin, (2) in the CRC4 mode, or if the framer (3) has automatic E-bit insertion enabled. Data in the Sa bit position is overwritten if any of the TCR.3–TCR.7 bits are set to 1. Please see the TCR register descriptions for more details.

Register Name: **RAF**
 Register Description: **Receive Align Frame Register**
 Register Address: **28 Hex**

| | | | | | | | | |
|-------|----|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

| NAME | BIT | FUNCTION |
|------|-----|----------------------------|
| Si | 7 | International Bit |
| 0 | 6 | Frame Alignment Signal Bit |
| 0 | 5 | Frame Alignment Signal Bit |
| 1 | 4 | Frame Alignment Signal Bit |
| 1 | 3 | Frame Alignment Signal Bit |
| 0 | 2 | Frame Alignment Signal Bit |
| 1 | 1 | Frame Alignment Signal Bit |
| 1 | 0 | Frame Alignment Signal Bit |

Register Name: **RNAF**
 Register Description: **Receive Nonalign Frame Register**
 Register Address: **29 Hex**

| | | | | | | | | |
|-------|----|---|---|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

| NAME | BIT | FUNCTION |
|------|-----|-------------------------------|
| Si | 7 | International Bit |
| 1 | 6 | Frame Nonalignment Signal Bit |
| A | 5 | Remote Alarm |
| Sa4 | 4 | Additional Bit 4 |
| Sa5 | 3 | Additional Bit 5 |
| Sa6 | 2 | Additional Bit 6 |
| Sa7 | 1 | Additional Bit 7 |
| Sa8 | 0 | Additional Bit 8 |

Register Name: **TAF**
 Register Description: **Transmit Align Frame Register**
 Register Address: **20 Hex**

| | | | | | | | | |
|-------|----|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Si | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Note: This register must be programmed with the 7-bit FAS word. The DS21Q59 does not automatically set these bits.

| NAME | BIT | FUNCTION |
|------|-----|--|
| Si | 7 | International Bit |
| 0 | 6 | Frame Alignment Signal Bit. Set this bit = 0. |
| 0 | 5 | Frame Alignment Signal Bit. Set this bit = 0. |
| 1 | 4 | Frame Alignment Signal Bit. Set this bit = 1. |
| 1 | 3 | Frame Alignment Signal Bit. Set this bit = 1. |
| 0 | 2 | Frame Alignment Signal Bit. Set this bit = 0. |
| 1 | 1 | Frame Alignment Signal Bit. Set this bit = 1. |
| 1 | 0 | Frame Alignment Signal Bit. Set this bit = 1. |

Register Name: **TNAF**
 Register Description: **Transmit Nonalign Frame Register**
 Register Address: **21 Hex**

| | | | | | | | | |
|-------|----|---|---|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | Si | 1 | A | Sa4 | Sa5 | Sa6 | Sa7 | Sa8 |

Note: Bit 6 must be programmed to 1. The DS21Q59 does not automatically set this bit.

| NAME | BIT | FUNCTION |
|------|-----|---|
| Si | 7 | International Bit |
| 1 | 6 | Frame Nonalignment Signal Bit. Set this bit = 1. |
| A | 5 | Remote Alarm (Used to transmit the alarm.) |
| Sa4 | 4 | Additional Bit 4 |
| Sa5 | 3 | Additional Bit 5 |
| Sa6 | 2 | Additional Bit 6 |
| Sa7 | 1 | Additional Bit 7 |
| Sa8 | 0 | Additional Bit 8 |

20. USER-CONFIGURABLE OUTPUTS

There are two user-configurable output pins for each transceiver, OUTA and OUTB. These pins can be programmed to output various clocks, alarms for line monitoring, or logic 0 and 1 levels to control external circuitry. They can also be used to access transmit data between the framer and transmit LIU. OUTA and OUTB can be active low or active high when operating as clock and alarm outputs. OUTA is active high if OUTAC.4 = 1 and active low if OUTAC.3 = 0. OUTB is active high if OUTBC.4 = 1 and active low if OUTBC.4 = 0 ([Table 20-A](#)). Select mode 0000 to control external circuitry. In this configuration, the OUTA pin follows OUTAC.4 and the OUTB pin follows OUTBC.4. The OUTAC register also contains a control bit for CMI operation. See [Section 22](#) for details about CMI operation.

Register Name: **OUTAC**
 Register Description: **OUTA Control Register**
 Register Address: **1A Hex**

| | | | | | | | | |
|-------|-------|------|------|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TTLIE | CMII | CMIE | OA4 | OA3 | OA2 | OA1 | OA0 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| TTLIE | 7 | TTL Input Enable. When this bit is set, the receiver can accept TTL positive and negative data at the RTIP and RRING inputs. The data is clocked in on the falling edge of MCLK. |
| CMII | 6 | CMI Invert. See Section 22 for details. 0 = CMI input data not inverted 1 = CMI input data inverted |
| CMIE | 5 | CMI Enable. See Section 22 for details. 0 = CMI disabled 1 = CMI enabled |
| OA4 | 4 | OUTA Control Bit 4. Inverts OUTA output. |
| OA3 | 3 | OUTA Control Bit 3. See Table 20-A for details. |
| OA2 | 2 | OUTA Control Bit 2. See Table 20-A for details. |
| OA1 | 1 | OUTA Control Bit 1. See Table 20-A for details. |
| OA0 | 0 | OUTA Control Bit 0. See Table 20-A for details. |

Register Name: **OUTBC**
 Register Description: **OUTB Control Register**
 Register Address: **1B Hex**

| | | | | | | | | |
|-------|------|---|---|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | NRZE | — | — | OB4 | OB3 | OB2 | OB1 | OB0 |

| NAME | BIT | FUNCTION |
|------|-----|---|
| NRZE | 7 | NRZ Enable. When this bit is set, the receiver can accept TTL-type NRZ data at the RTIP input. RRING becomes a clock input. 0 = RTIP and RRING are in normal mode. 1 = RTIP becomes an NRZ TTL-type input and RRING is its associated clock input. Data at RTIP is clocked in on the falling edge of the clock present on RRING. |
| — | 6 | Unused. Should be set = 0 for proper operation. |
| — | 5 | Unused. Should be set = 0 for proper operation. |
| OB4 | 4 | OUTB Control Bit 4. Inverts OUTB output. |
| OB3 | 3 | OUTB Control Bit 3 |
| OB2 | 2 | OUTB Control Bit 2 |
| OB1 | 1 | OUTB Control Bit 1 |
| OB0 | 0 | OUTB Control Bit 0 |

Table 20-A. OUTA and OUTB Function Select

| OA3 OB3 | OA2 OB2 | OA1 OB1 | OA0 OB0 | FUNCTION |
|------------|------------|------------|------------|--|
| 0 | 0 | 0 | 0 | External Hardware Control Bit. In this mode, OUTA and OUTB can be used as simple control pins for external circuitry. Use OA4 and OB4 to toggle OUTA and OUTB. |
| 0 | 0 | 0 | 1 | RCLK. Receive recovered clock. |
| 0 | 0 | 1 | 0 | Receive Loss-of-Sync Indicator. Real-time hardware version of SR1.0 (Table 9-A). |
| 0 | 0 | 1 | 1 | Receive Loss-of-Carrier Indicator. Real-time hardware version of SR1.1 (Table 9-A). |
| 0 | 1 | 0 | 0 | Receive Remote Alarm Indicator. Real-time hardware version of SR1.2 (Table 9-A). |
| 0 | 1 | 0 | 1 | Receive Unframed All-Ones Indicator. Real-time hardware version of SR1.3 (Table 9-A). |
| 0 | 1 | 1 | 0 | Receive Slip-Occurrence Indicator. One-clock-wide pulse for every slip of the receive elastic store. Hardware version of SR1.4. |
| 0 | 1 | 1 | 1 | Receive CRC Error Indicator. One-clock-wide pulse for every multiframe that contains a CRC error. Output forced to 0 during loss of sync. |
| 1 | 0 | 0 | 0 | Loss-of-Transmit Clock Indicator. Real-time hardware version SR2.2 (Table 9-A). |
| 1 | 0 | 0 | 1 | RFSYNC. Recovered frame-sync pulse. |
| 1 | 0 | 1 | 0 | PRBS Bit Error. A half-clock-wide pulse for every bit error in the received PRBS pattern. |
| 1 | 0 | 1 | 1 | TDATA/RDATA. OUTB outputs an NRZ version of the transmit data stream (TDATA) prior to the transmit line interface. OUTA outputs the received serial data stream (RDATA) prior to the elastic store. |
| 1 | 1 | 0 | 0 | Receive CRC4 Multiframe Sync. Recovered CRC4 MF sync pulse. |
| 1 | 1 | 0 | 1 | Receive CAS Multiframe Sync. Recovered CAS MF sync pulse. |
| 1 | 1 | 1 | 0 | Transmit Current Limit. Real-time indicator that the TTIP and TRING outputs have reached their 50mA current limit. |
| 1 | 1 | 1 | 1 | TPOS/TNEG Output. This mode outputs the AMI/HDB3 encoded transmit data. OUTA outputs TNEG data. OUTB outputs TPOS data. |

21. LINE INTERFACE UNIT

The line interface unit contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the E1 line; and the jitter attenuator. The line interface control register (LICR), described below, controls each of these three sections.

Register Name: **LICR**
 Register Description: **Line Interface Control Register**
 Register Address: **17 Hex**

| | | | | | | | | |
|-------|----|----|----|-----|-----|-------|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | L2 | L1 | L0 | EGL | JAS | JABDS | DJA | TPD |

| NAME | BIT | FUNCTION |
|-------|-----|--|
| L2 | 7 | Line Build-Out Select Bit 2. Sets the transmitter build-out. |
| L1 | 6 | Line Build-Out Select Bit 1. Sets the transmitter build-out. |
| L0 | 5 | Line Build-Out Select Bit 0. Sets the transmitter build-out. |
| EGL | 4 | Receive Equalizer Gain Limit 0 = -12dB 1 = -43dB |
| JAS | 3 | Jitter Attenuator Select 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side |
| JABDS | 2 | Jitter Attenuator Buffer Depth Select 0 = 128 bits 1 = 32 bits (use for delay-sensitive applications) |
| DJA | 1 | Disable Jitter Attenuator 0 = jitter attenuator enabled 1 = jitter attenuator disabled |
| TPD | 0 | Transmit Power-Down 0 = powers down the transmitter and tri-states the TTIP and TRING pins 1 = normal transmitter operation |

21.1 Receive Clock and Data Recovery

The DS21Q59 contains a digital clock recovery system. (See [Figure 3-1](#) and [Figure 21-1](#) for more details.) The device couples to the receive E1 shielded twisted pair or coax through a 1:1 transformer ([Table 21-B](#)). The 2.048MHz clock attached at the MCLK pin is internally multiplied by 16 through an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler, which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance ([Figure 21-4](#)).

Normally, RCLK is the recovered clock from the E1 AMI/HDB3 waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, an RCL condition occurs and the RCLK is sourced from the clock applied at the MCLK pin. If the jitter attenuator is either placed in the transmit path or is disabled, RCLK can exhibit slightly shorter high cycles of the clock. This is because of the highly oversampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. See *Receive AC Characteristics* in Section [26.4](#) for more details.

21.1.1 Termination

The DS21Q59 is designed to be fully software-selectable for 75Ω and 120Ω termination without the need to change any external resistors. The user can configure the DS21Q59 for 75Ω or 120Ω receive termination by setting the IRTSEL (CCR5.4) bit. When using the internal termination feature, the external termination resistance should be 120Ω (typically two 60Ω resistors). Setting IRTSEL = 1 causes the DS21Q59 to internally apply parallel resistance to the external resistors to adjust the termination to 75Ω ([Figure 21-2](#)).

21.2 Transmit Waveshaping and Line Driving

The DS21Q59 uses a set of laser-trimmed delay lines and a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the E1 line. The waveforms meet the ITU G.703 specifications (Figure 21-3). The user selects which waveform is to be generated by properly programming the L2/L1/L0 bits in the line interface control register (LICR). The DS21Q59 can be set up in a number of various configurations depending on the application (Table 21-A).

Table 21-A. Line Build-Out Select in LICR

| L2 | L1 | L0 | APPLICATION | TRANSFORMER | RETURN LOSS* | Rt (Ω)** |
|----|----|----|--|-------------|--------------|-------------------|
| 0 | 0 | 0 | 75 Ω normal | 1:2 step-up | N.M. | 0 |
| 0 | 0 | 1 | 120 Ω normal | 1:2 step-up | N.M. | 0 |
| 0 | 1 | 0 | 75 Ω with protection resistors | 1:2 step-up | N.M. | 2.5 |
| 0 | 1 | 1 | 120 Ω with protection resistors | 1:2 step-up | N.M. | 2.5 |
| 1 | 0 | 0 | 75 Ω with high return loss | 1:2 step-up | 21dB | 6.2 |
| 1 | 0 | 1 | 120 Ω with high return loss | 1:2 step-up | 21dB | 11.6 |

*N.M. = Not meaningful (return loss value too low for significance)

**See Application Note 336: Transparent Operation on T1, E1 Framers and Transceivers for details on E1 line interface design.

Because of the nature of the transmitter's design, very little jitter (less than $0.005U_{I,P,P}$ broadband from 10Hz to 100kHz) is added to the jitter present on TCLK (or source used for transmit clock). Also, the waveform created is independent of the duty cycle of TCLK. The transmitter in the device couples to the E1 transmit-shielded twisted pair or coax through a 1:2 step-up transformer, as shown in Figure 21-1. For the devices to create the proper waveforms, the transformer used must meet the specifications listed in Table 21-B. The line driver in the device contains a current limiter that prevents more than 50mA (RMS) from being sourced in a 1 Ω load.

Table 21-B. Transformer Specifications

| SPECIFICATION | RECOMMENDED VALUE |
|--------------------------|---|
| Turns Ratio | 1:1 (receive) and 1:2 (transmit) \pm 3% |
| Primary Inductance | 600 μ H minimum |
| Leakage Inductance | 1.0 μ H maximum |
| Intertwining Capacitance | 40pF maximum |
| DC Resistance | 1.2 Ω maximum |

Figure 21-1. External Analog Connections (Basic Configuration)

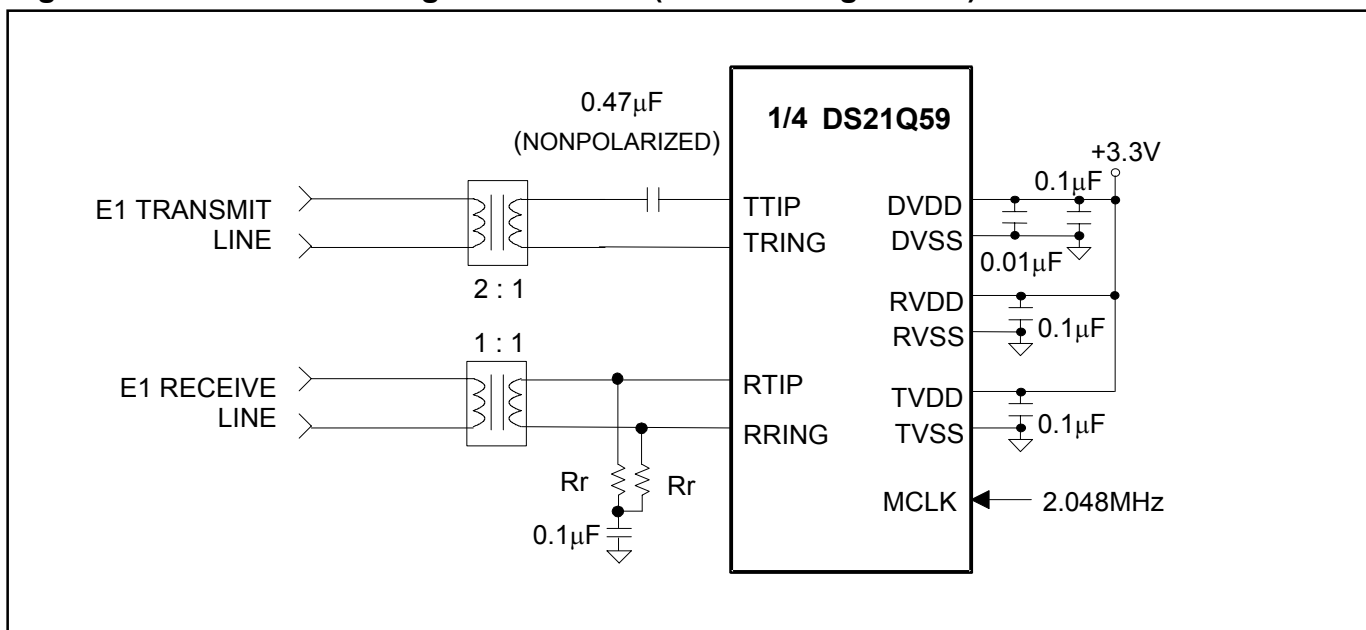


Figure 21-2. External Analog Connections (Protected Interface)

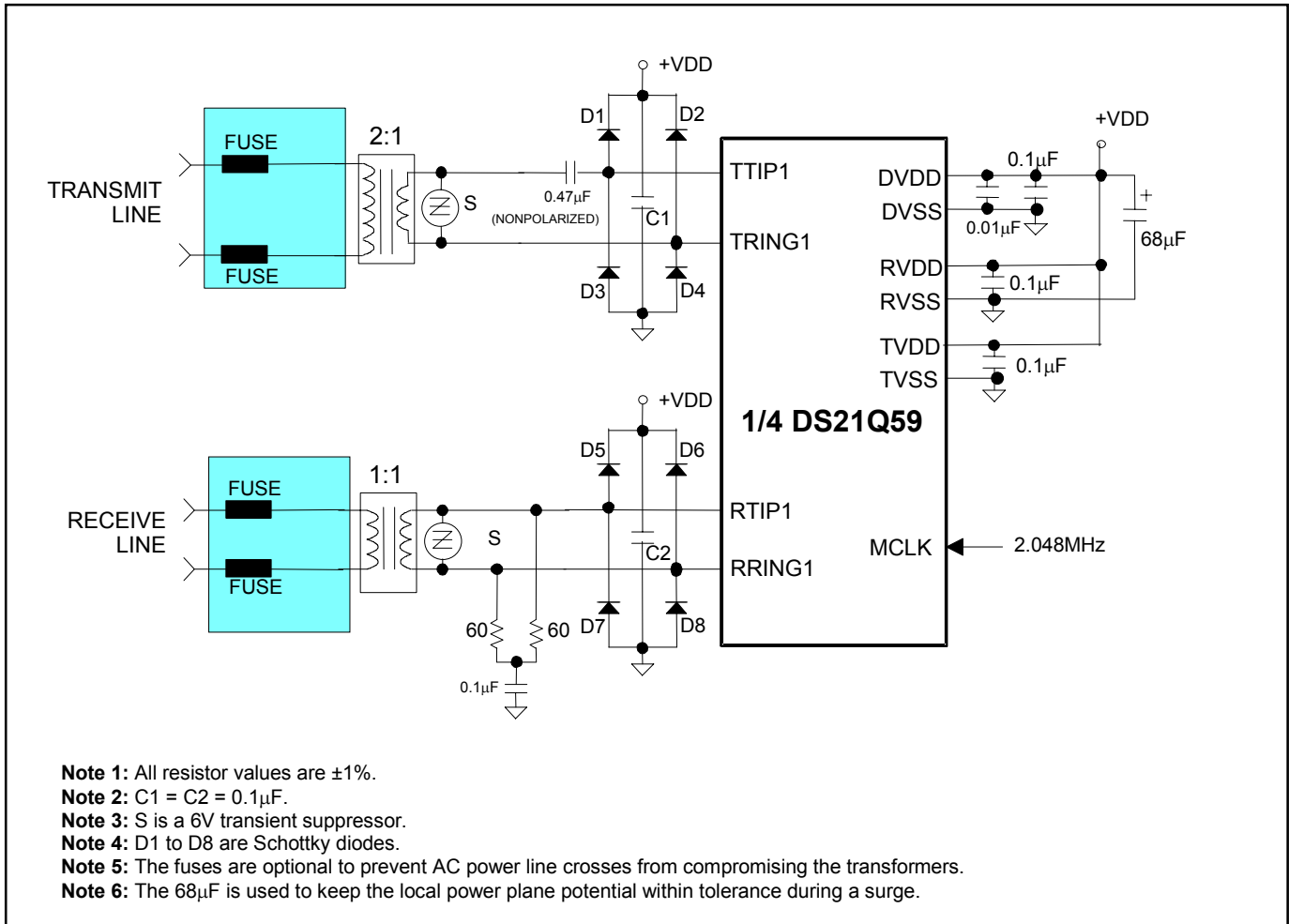
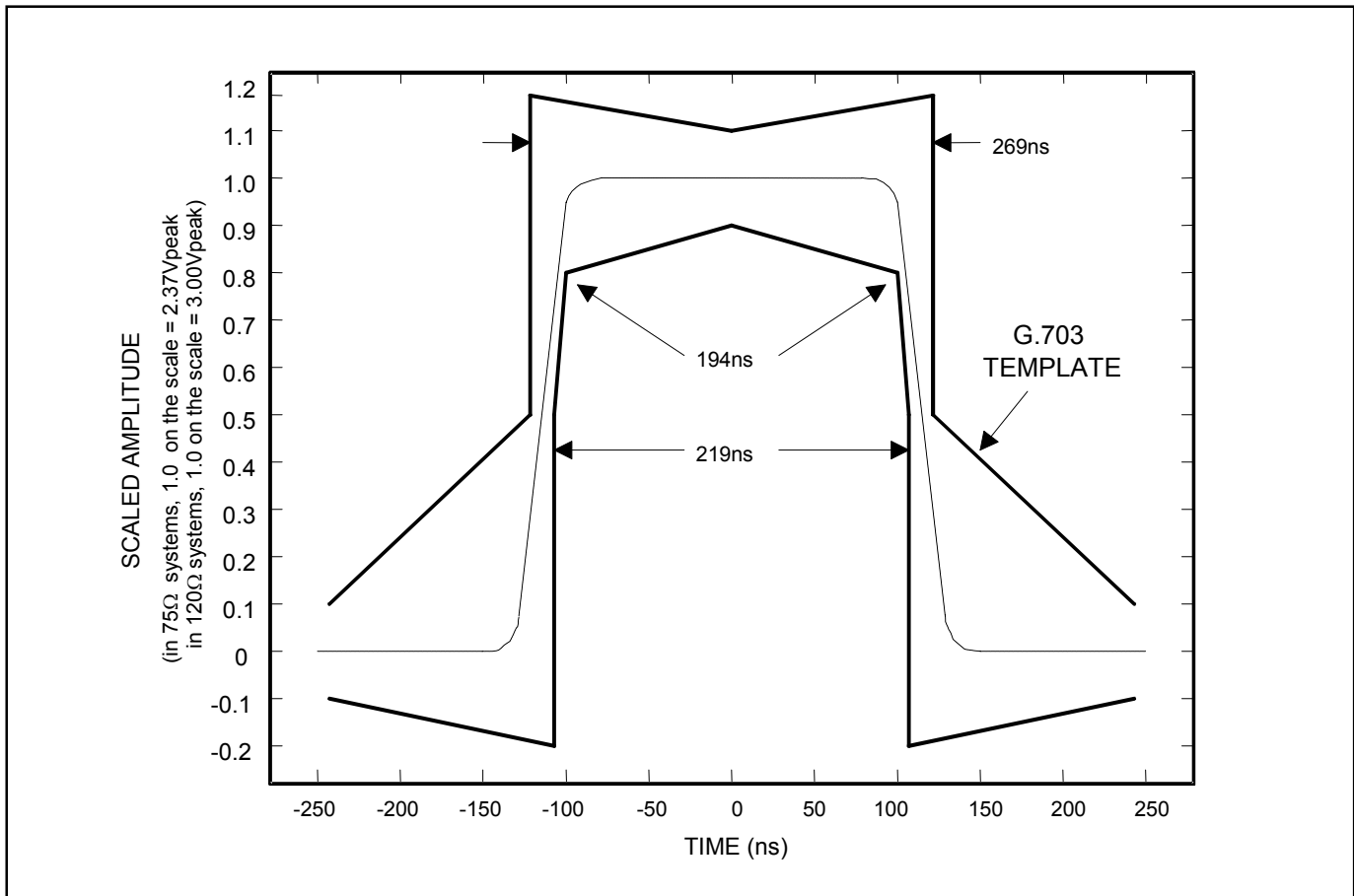


Figure 21-3. Transmit Waveform Template

21.3 Jitter Attenuators

The DS21Q59 contains an on-board clock and data jitter attenuator for each transceiver and a single, undedicated “clock only” jitter attenuator. This undedicated jitter attenuator is shown in the block diagram (Figure 3-1) as the alternate jitter attenuator.

21.3.1 Clock and Data Jitter Attenuators

The clock and data jitter attenuators can be mapped into the receive or transmit paths and can be set to buffer depths of either 32 or 128 bits through the LICR. The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications. The characteristics of the attenuators are shown in Figure 21-5. The jitter attenuators can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, setting the DJA bit in the LICR can disable the jitter attenuator (in effect, remove it). For the jitter attenuator to operate properly, a 2.048MHz clock (± 50 ppm) must be applied at the MCLK pin. On-board circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKI pin to create a smooth jitter-free clock that is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKI pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either $120U_{I,P,P}$ (buffer depth is 128 bits) or $28U_{I,P,P}$ (buffer depth is 32 bits), the DS21Q59 divides the internal nominal 32.768MHz clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the jitter attenuator limit trip (JALT) bit in the receive information register (RIR.5).

21.3.2 Undedicated Clock Jitter Attenuator

The undedicated jitter attenuator is useful for preparing a user-supplied clock for use as a transmission clock (TCLK). AJACKI is the input pin and AJCAKO is the output pin. Clocks generated by certain types of PLL or other synthesizers can contain too much jitter to be appropriate for transmission. Network requirements limit the amount of jitter that can be transmitted onto the network. This feature is enabled by setting SC1CR.7 = 1 in Transceiver 1.

Figure 21-4. Jitter Tolerance

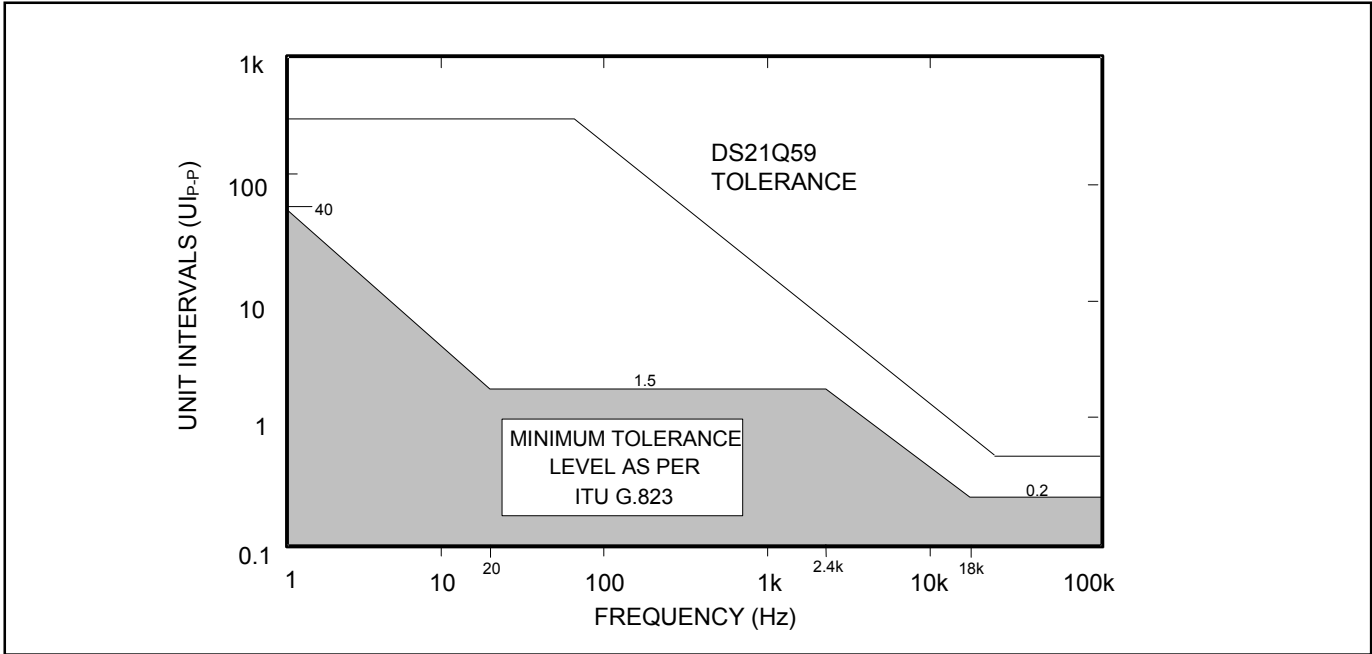
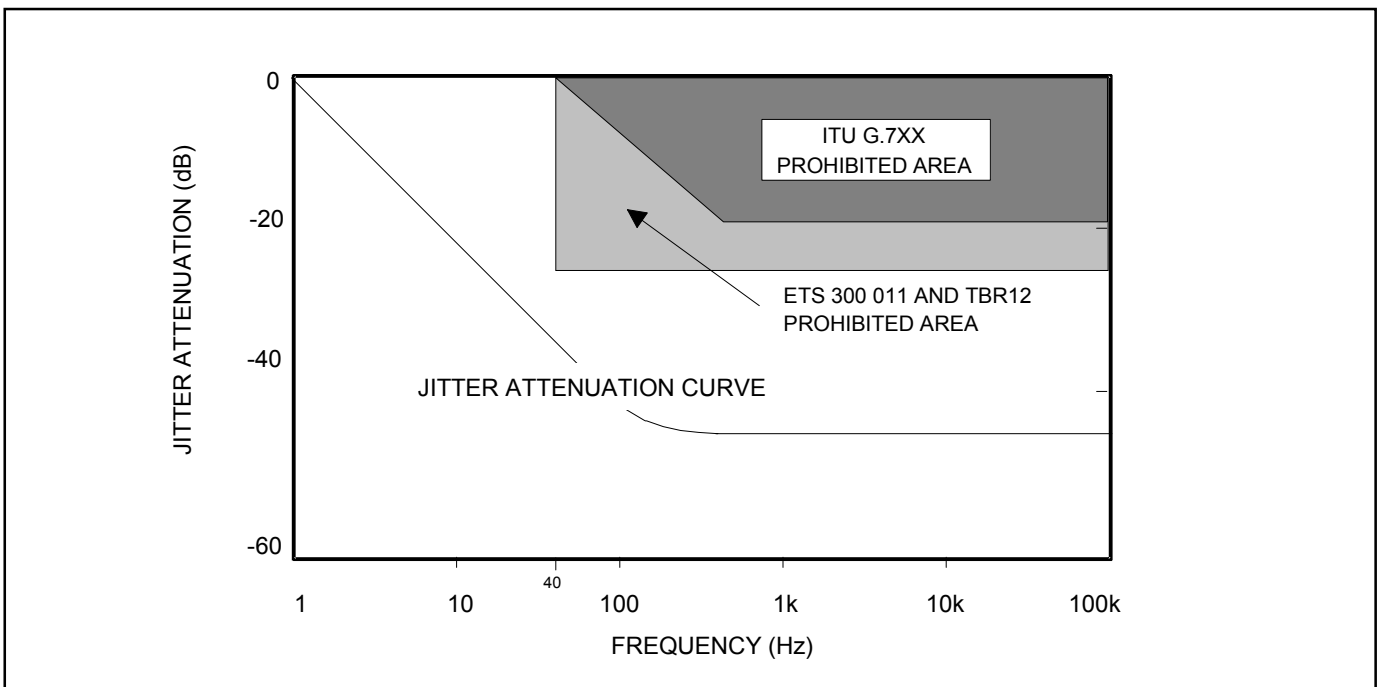


Figure 21-5. Jitter Attenuation



22. CODE MARK INVERSION (CMI)

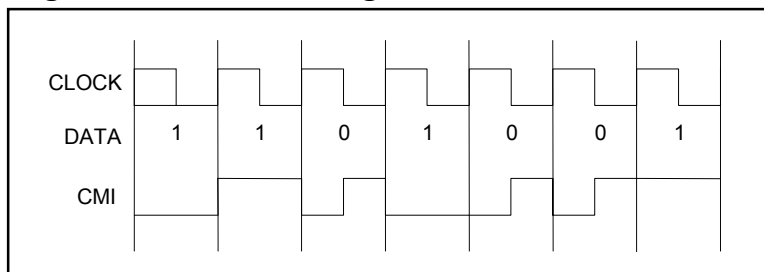
The DS21Q59 provides a CMI interface for connecting to optical transports. This interface is a unipolar 1T2B-coded signal. Ones are alternately encoded as a logical 1 or 0 level for the full duration of the clock period. Zeros are encoded as a 0-to-1 transition at the middle of the clock period. [Figure 22-1](#) shows an example data pattern and its CMI result. The control bit for enabling CMI is in the OUTAC register, as shown below.

Register Name: **OUTAC**
 Register Description: **OUTA Control Register**
 Register Address: **1A Hex**

| | | | | | | | | |
|-------|-------|------|------|-----|-----|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | TTLIE | CMII | CMIE | OA4 | OA3 | OA2 | OA1 | OA0 |

| NAME | BIT | FUNCTION |
|-------|-----|---|
| TTLIE | 7 | TTL Input Enable. When this bit is set, the receiver can accept TTL positive and negative data at the RTIP and RRING inputs. The data is clocked in on the falling edge of MCLK. |
| CMII | 6 | CMI Invert 0 = CMI input data not inverted 1 = CMI input data inverted |
| CMIE | 5 | Transmit and Receive CMI Enable 0 = Transmit and receive line interface operates in normal AMI/HDB3 mode 1 = Transmit and receive line interface operate in CMI mode. TTIP is CMI output and RTIP is CMI input. In this mode of operation TRING and RRING are no connects. |
| OA4 | 4 | OUTA Control Bit 4. Inverts OUTA output. |
| OA3 | 3 | OUTA Control Bit 3. See Table 20-A for details. |
| OA2 | 2 | OUTA Control Bit 2. See Table 20-A for details. |
| OA1 | 1 | OUTA Control Bit 1. See Table 20-A for details. |
| OA0 | 0 | OUTA Control Bit 0. See Table 20-A for details. |

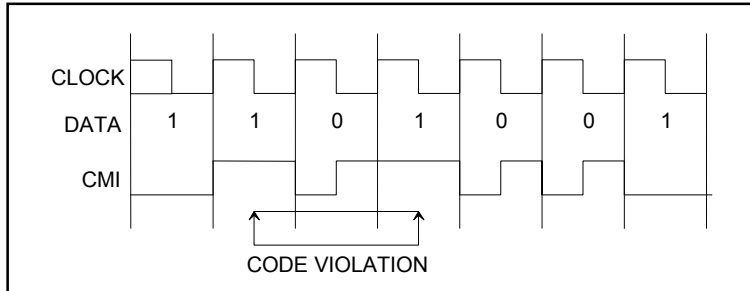
Figure 22-1. CMI Coding



Transmit and receive CMI is enabled through OUTAC.7. When this register bit is set, the TTIP pin outputs CMI-coded data at normal TTL-type levels. This signal can be used to directly drive an optical interface. When CMI is enabled, the user can also use HDB3 coding.

When this register bit is set, the RTIP pin becomes a unipolar CMI input. The CMI signal is processed to extract and align the clock with data. The bipolar code-violation counter counts CVs in the CMI signal. CVs are defined as consecutive 1s of the same polarity, as shown in [Figure 22-2](#). If HDB3 precoding is enabled, the CVs generated by HDB3 are not counted as errors.

Figure 22-2. Example of CMI Code Violation



23. INTERLEAVED PCM BUS OPERATION

In many architectures, the PCM outputs of individual framers are combined into higher-speed PCM buses to simplify transport across the system backplane. The DS21Q59 can be configured to allow PCM data buses to be multiplexed into higher-speed data buses, eliminating external hardware and saving board space and cost. The DS21Q59 uses a channel interleave method. See [Figure 24-4](#) and [Figure 24-7](#) for details of the channel interleave.

The interleaved PCM bus option supports three bus speeds. The 4.096MHz bus speed allows two PCM data streams to share a common bus. The 8.192MHz bus speed allows four PCM data streams to share a common bus. The 16.384MHz bus speed allows eight PCM data streams to share a common bus. See [Figure 23-1](#) for an example of four transceivers sharing a common 8.192MHz PCM bus. The receive elastic stores of each transceiver must be enabled. Through the IBO register the user can configure each transceiver for a specific bus speed and position. For all IBO bus configurations each transceiver is assigned an exclusive position in the high-speed PCM bus. When the device is configured for IBO operation, the TSYNCx pin should be configured as an output or as an input connected to ground. The user cannot supply a TSYNCx signal in this mode. When IBO operation is enabled, TSYNCx will be internally tied to RSYNCx. If TSYNCx is configured as an input, the physical pin will be disconnected from the internal TSYNCx signal and should therefore be connected to ground to keep it from floating.

Register Name: **IBO**
 Register Description: **Interleave Bus Operation Register**
 Register Address: **1C Hex**

| | | | | | | | | |
|-------|---|--------|------|------|-------|-----|-----|-----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | — | IBOTCS | SCS1 | SCS0 | IBOEN | DA2 | DA1 | DA0 |

| NAME | BIT | FUNCTION |
|--------|-----|---|
| — | 7 | Not Assigned. Should be set to 0. |
| IBOTCS | 6 | IBO Transmit Clock Source 0 = TCLK pin is the source of transmit clock 1 = Transmit clock is internally derived from the clock at the SYSCLK pin |
| SCS1 | 5 | System Clock Select Bit 1 (Table 23-A) |
| SCS0 | 4 | System Clock Select Bit 0 (Table 23-A) |
| IBOEN | 3 | Interleave Bus Operation Enable 0 = IBO disabled 1 = IBO enabled |
| DA2 | 2 | Device Assignment Bit 3 (Table 23-B) |
| DA1 | 1 | Device Assignment Bit 2 (Table 23-B) |
| DA0 | 0 | Device Assignment Bit 1 (Table 23-B) |

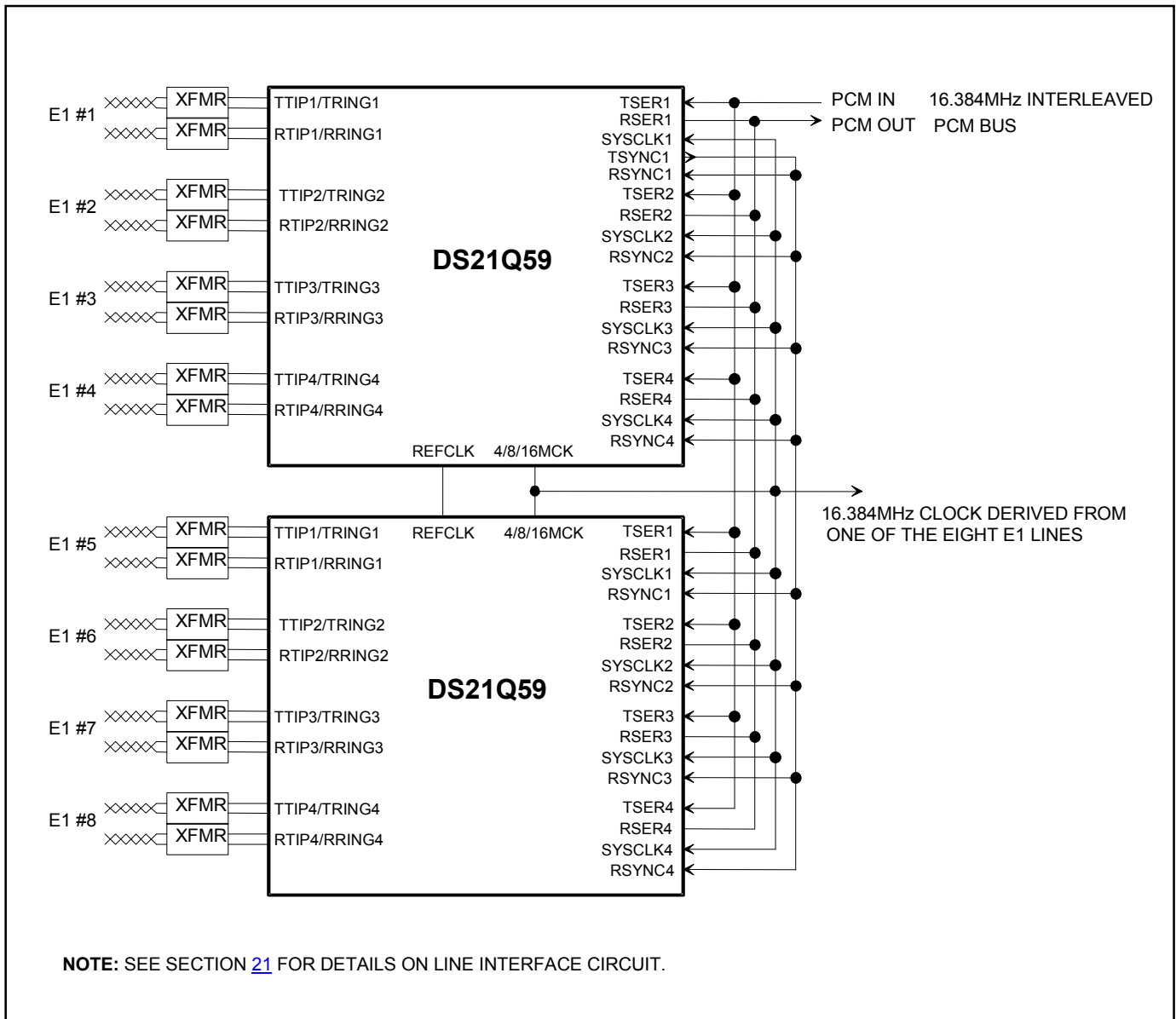
Table 23-A. IBO System Clock Select

| SCS1 | SCS0 | FUNCTION |
|------|------|---------------------------------|
| 0 | 0 | 2.048MHz, single device on bus |
| 0 | 1 | 4.096MHz, two devices on bus |
| 1 | 0 | 8.192MHz, four devices on bus |
| 1 | 1 | 16.384MHz, eight devices on bus |

Table 23-B. IBO Device Assignment

| DA2 | DA1 | DA0 | FUNCTION |
|-----|-----|-----|-------------------|
| 0 | 0 | 0 | 1st device on bus |
| 0 | 0 | 1 | 2nd device on bus |
| 0 | 1 | 0 | 3rd device on bus |
| 0 | 1 | 1 | 4th device on bus |
| 1 | 0 | 0 | 5th device on bus |
| 1 | 0 | 1 | 6th device on bus |
| 1 | 1 | 0 | 7th device on bus |
| 1 | 1 | 1 | 8th device on bus |

Figure 23-1. IBO Configuration Using Two DS21Q59 Transceivers (Eight E1 Lines)



24. FUNCTIONAL TIMING DIAGRAMS

24.1 Receive

Figure 24-1. Receive Frame and Multiframe Timing

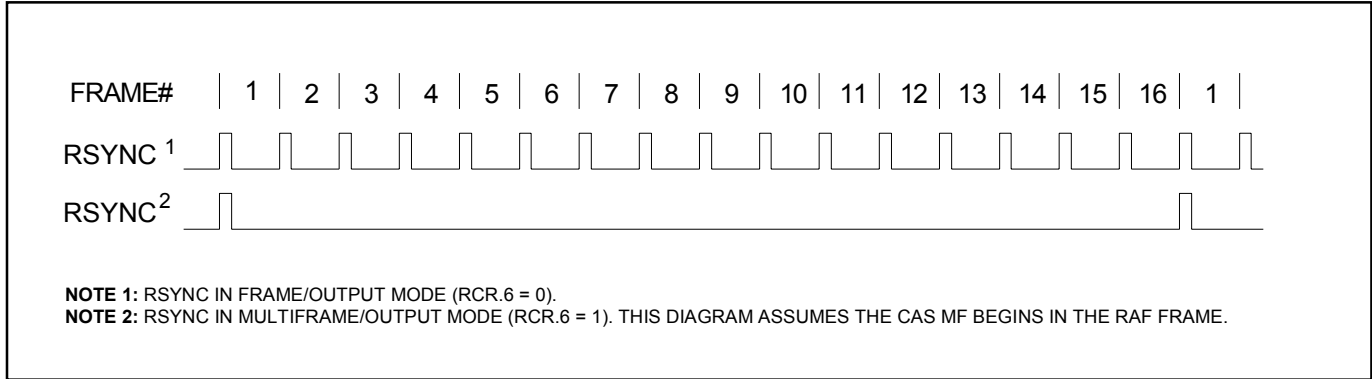


Figure 24-2. Receive Boundary Timing (With Elastic Store Disabled)

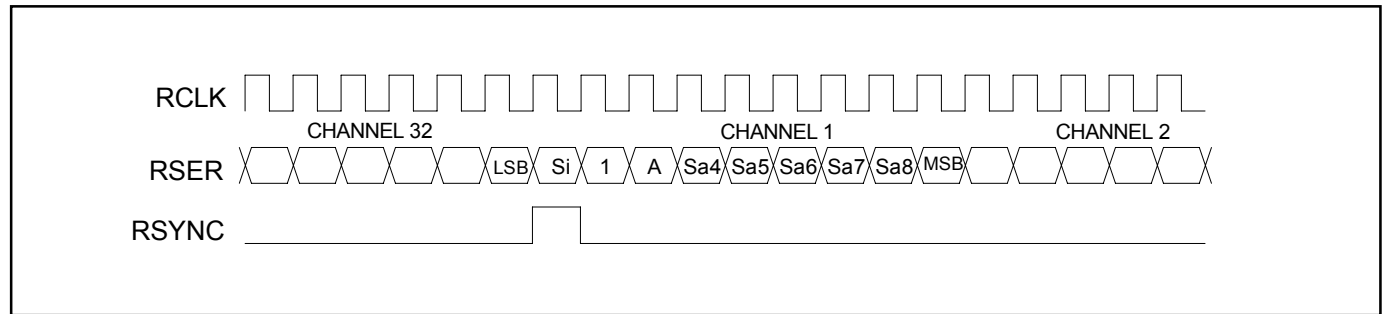


Figure 24-3. Receive Boundary Timing (With Elastic Store Enabled)

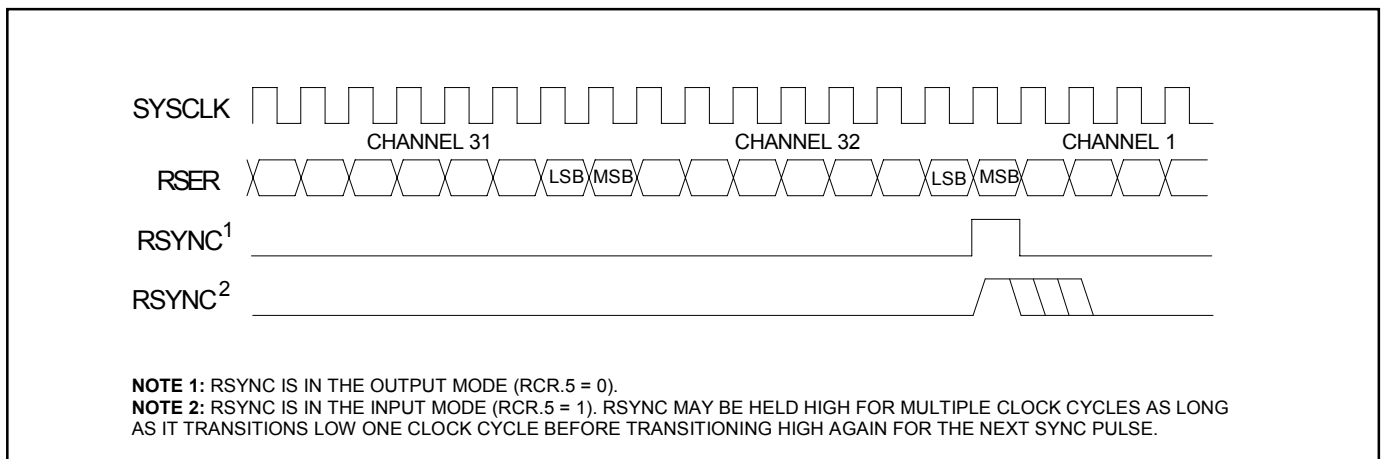
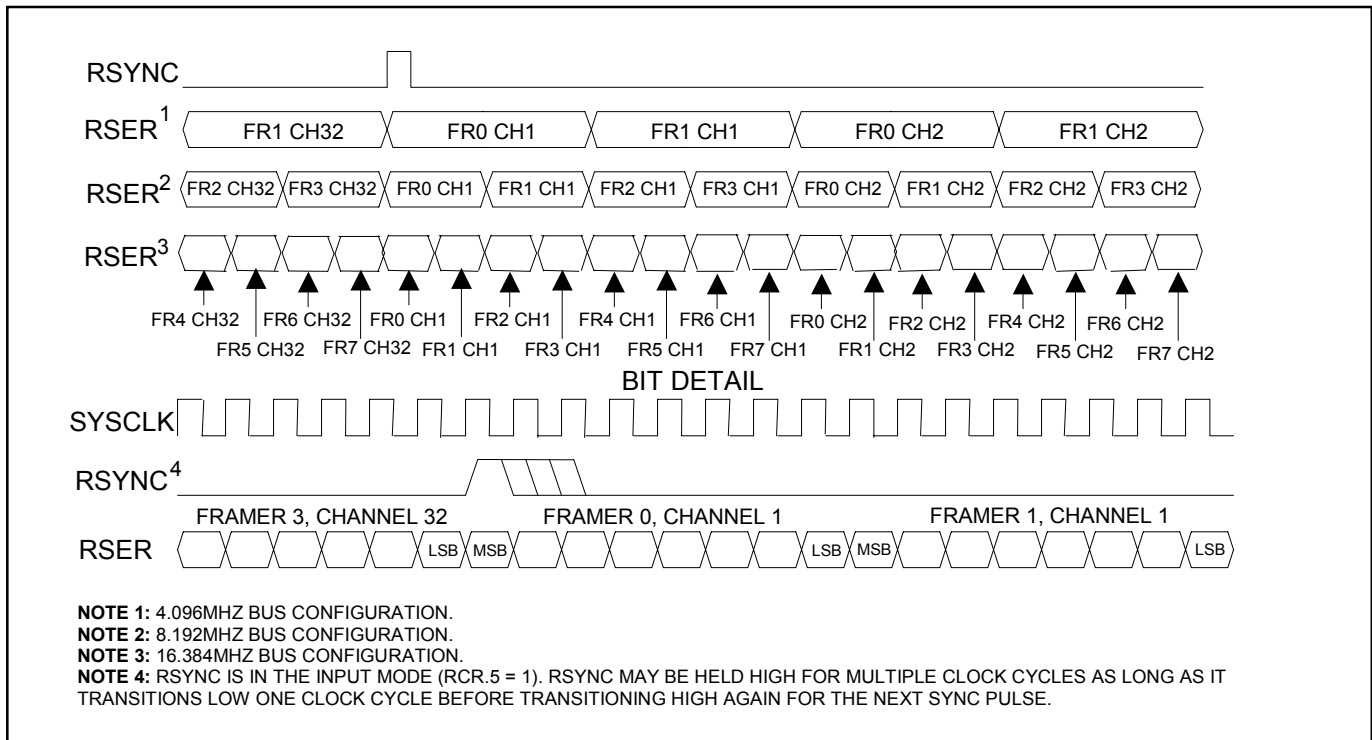


Figure 24-4. Receive Interleave Bus Operation



24.2 Transmit

Figure 24-5. Transmit Frame and Multiframe Timing

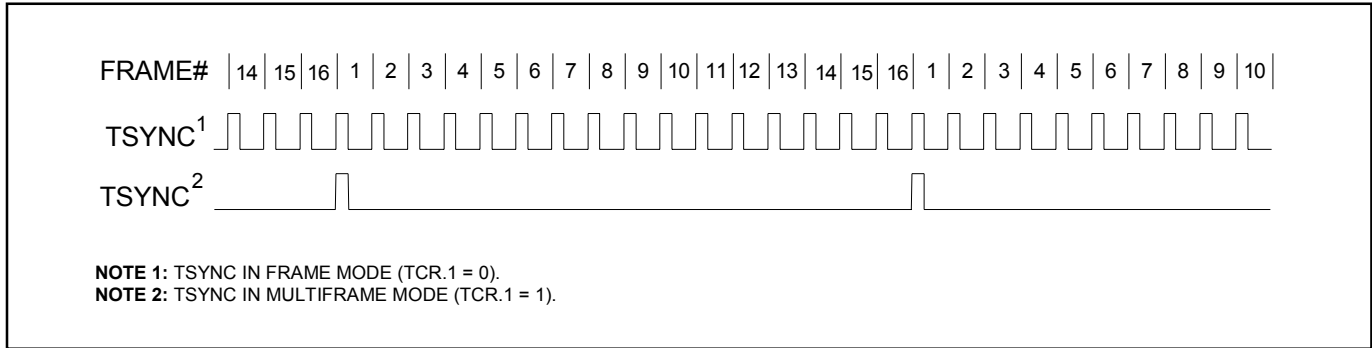


Figure 24-6. Transmit Boundary Timing

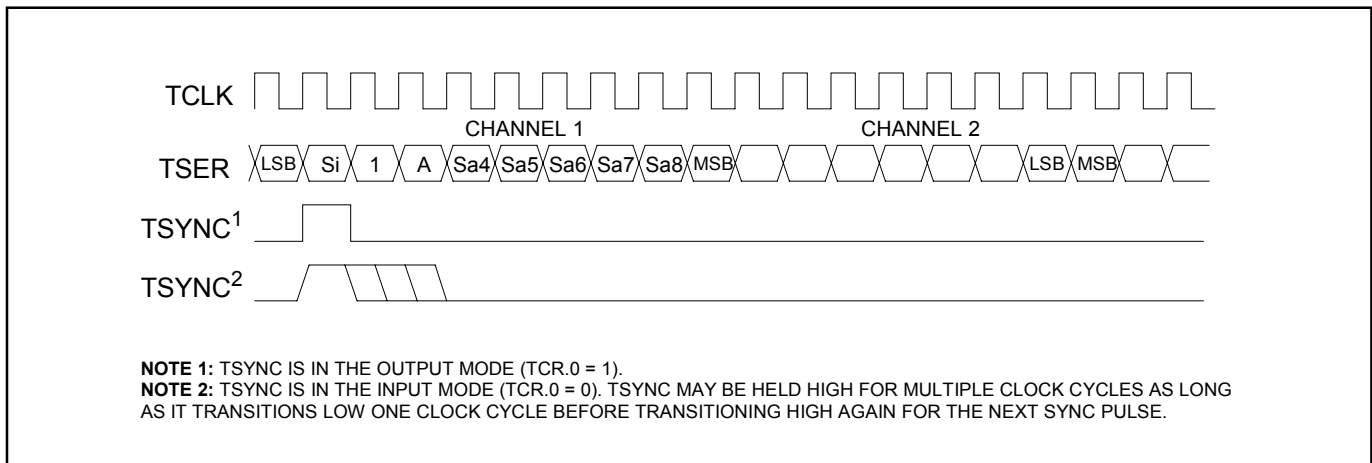


Figure 24-7. Transmit Interleave Bus Operation

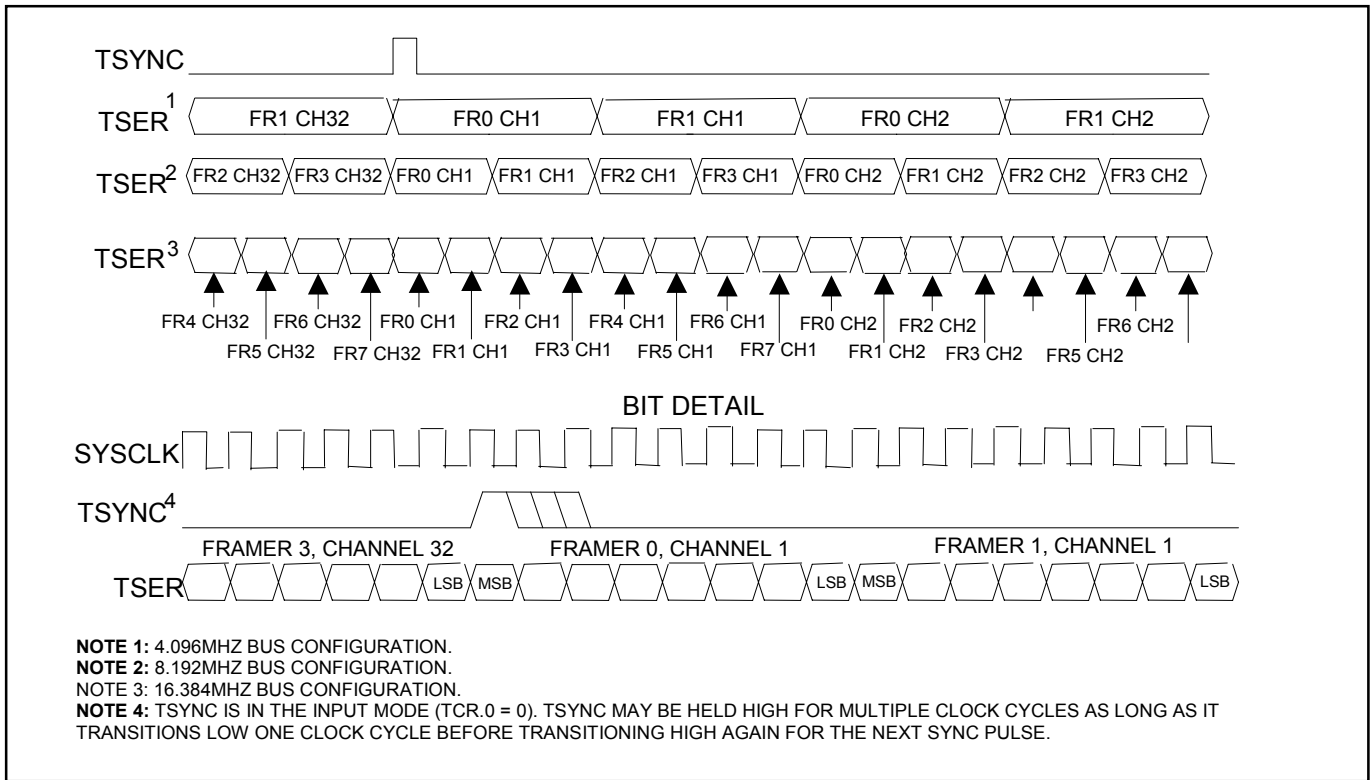


Figure 24-8. Framer Synchronization Flowchart

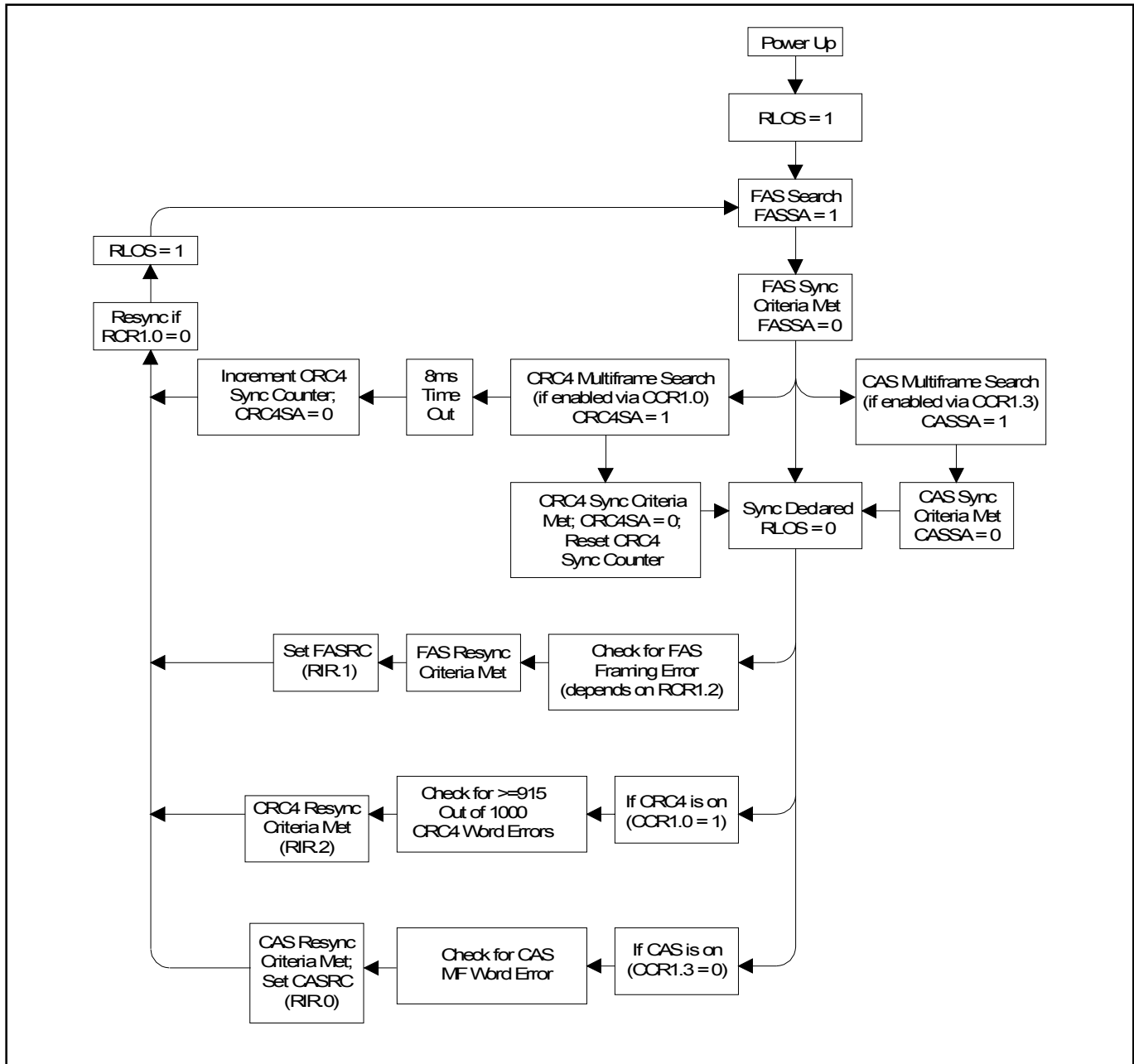
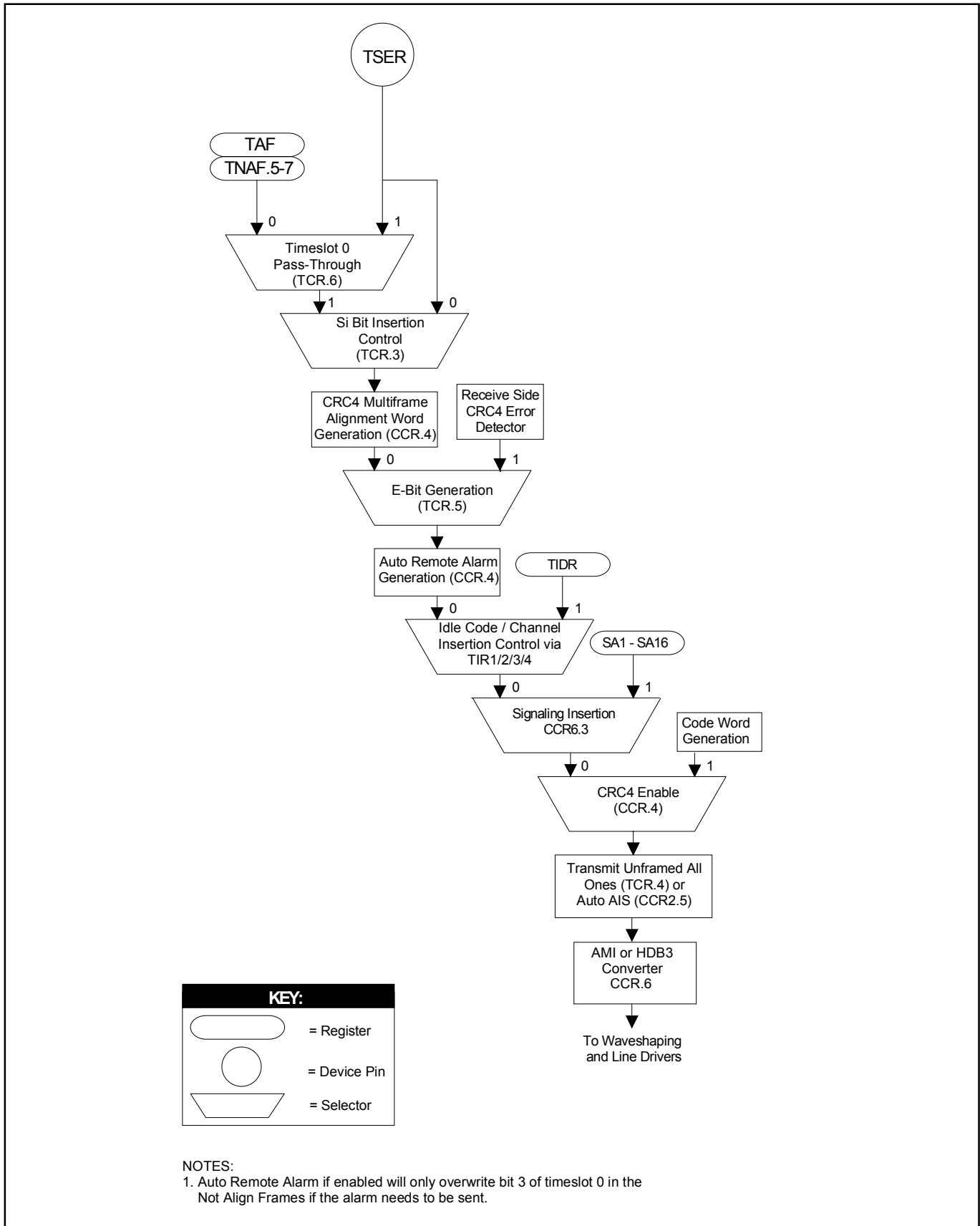


Figure 24-9. Transmit Data Flow



25. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| Voltage Range on Any Pin Relative to Ground | -1.0V to +6.0V |
| Operating Temperature Range for DS21Q59L | 0°C to +70°C |
| Operating Temperature Range for DS21Q59LN | -40°C to +85°C |
| Storage Temperature Range | -55°C to +125°C |
| Soldering Temperature Range | See IPC/JEDEC J-STD-020A Specification |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

RECOMMENDED DC OPERATING CONDITIONS

($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for DS21Q59L; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS21Q59LN.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|----------|------------|-------|-----|-------|-------|
| Logic 1 | V_{IH} | | 2.0 | | 5.5 | V |
| Logic 0 | V_{IL} | | -0.3 | | +0.8 | V |
| Supply | V_{DD} | (Note 1) | 3.135 | 3.3 | 3.465 | V |

CAPACITANCE

($T_A = +25^\circ\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|-----------|------------|-----|-----|-----|-------|
| Input Capacitance | C_{IN} | | | 5 | | pF |
| Output Capacitance | C_{OUT} | | | 7 | | pF |

DC CHARACTERISTICS

($V_{DD} = 3.3\text{V} \pm 5\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for DS21Q59L; $V_{DD} = 3.3\text{V} \pm 5\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for DS21Q59LN.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------|----------|------------|------|-----|------|---------------|
| Supply Current at 3.3V | I_{DD} | (Note 2) | | 230 | | mA |
| Input Leakage | I_{IL} | (Note 3) | -1.0 | | +1.0 | μA |
| Output Leakage | I_{LO} | (Note 4) | | | +1.0 | μA |
| Output Current (2.4V) | I_{OH} | | -1.0 | | | mA |
| Output Current (0.4V) | I_{OL} | | +4.0 | | | mA |

Note 1: Applies to RVDD, TVDD, and DVDD.

Note 2: $TCLKs = SYSCLKs = MCLK = 2.048\text{MHz}$; outputs open circuited; TTIPs and TRINGs driving 30Ω ; QRSS data pattern.
 $0.0\text{V} < V_{IN} < V_{DD}$.

Note 3: Applied to $\overline{\text{INT}}$ when tri-stated.

Note 4: Applies to output pins in a tri-state condition.

26. AC TIMING PARAMETERS AND DIAGRAMS

26.1 Multiplexed Bus AC Characteristics

Table 26-A. AC Characteristics—Multiplexed Parallel Port

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)
([Figure 26-1](#), [Figure 26-2](#), and [Figure 26-3](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------|------------|-----|-----|-----|-------|
| Cycle Time | t_{CYC} | | 200 | | | ns |
| Pulse Width, DS Low or \overline{RD} High | PW_{EL} | | 100 | | | ns |
| Pulse Width, DS High or \overline{RD} Low | PW_{EH} | | 100 | | | ns |
| Input Rise/Fall times | t_R, t_F | | | | 20 | ns |
| R/\overline{W} Hold Time | t_{RWH} | | 10 | | | ns |
| R/\overline{W} Setup Time Before DS High | t_{RWS} | | 50 | | | ns |
| \overline{CS} Setup Time Before DS, \overline{WR} , or \overline{RD} Active | t_{CS} | | 20 | | | ns |
| \overline{CS} Hold Time | t_{CH} | | 0 | | | ns |
| Read Data Hold Time | t_{DHR} | | 10 | | 50 | ns |
| Write Data Hold Time | t_{DHW} | | 0 | | | ns |
| Muxed Address Valid to AS or ALE Fall | t_{ASL} | | 15 | | | ns |
| Muxed Address Hold Time | t_{AHL} | | 10 | | | ns |
| Delay Time DS, \overline{WR} , or \overline{RD} to AS or ALE Rise | t_{ASD} | | 20 | | | ns |
| Pulse Width AS or ALE High | PW_{ASH} | | 30 | | | ns |
| Delay Time, AS or ALE to DS, \overline{WR} , or \overline{RD} | t_{ASED} | | 10 | | | ns |
| Output Data-Delay Time from DS or \overline{RD} | t_{DDR} | | 20 | | 140 | ns |
| Data Setup Time | t_{DSW} | | 50 | | | ns |

Figure 26-1. Intel Bus Read AC Timing (PBTS = 0)

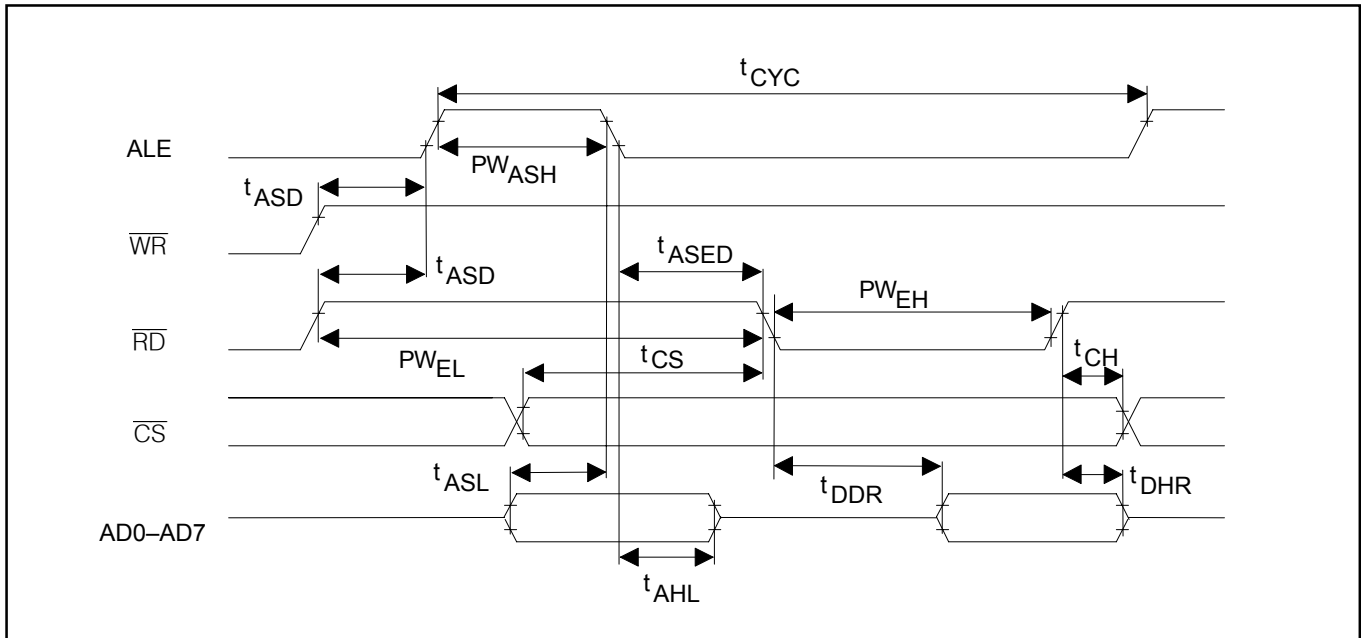


Figure 26-2. Intel Bus Write Timing (PBTS = 0)

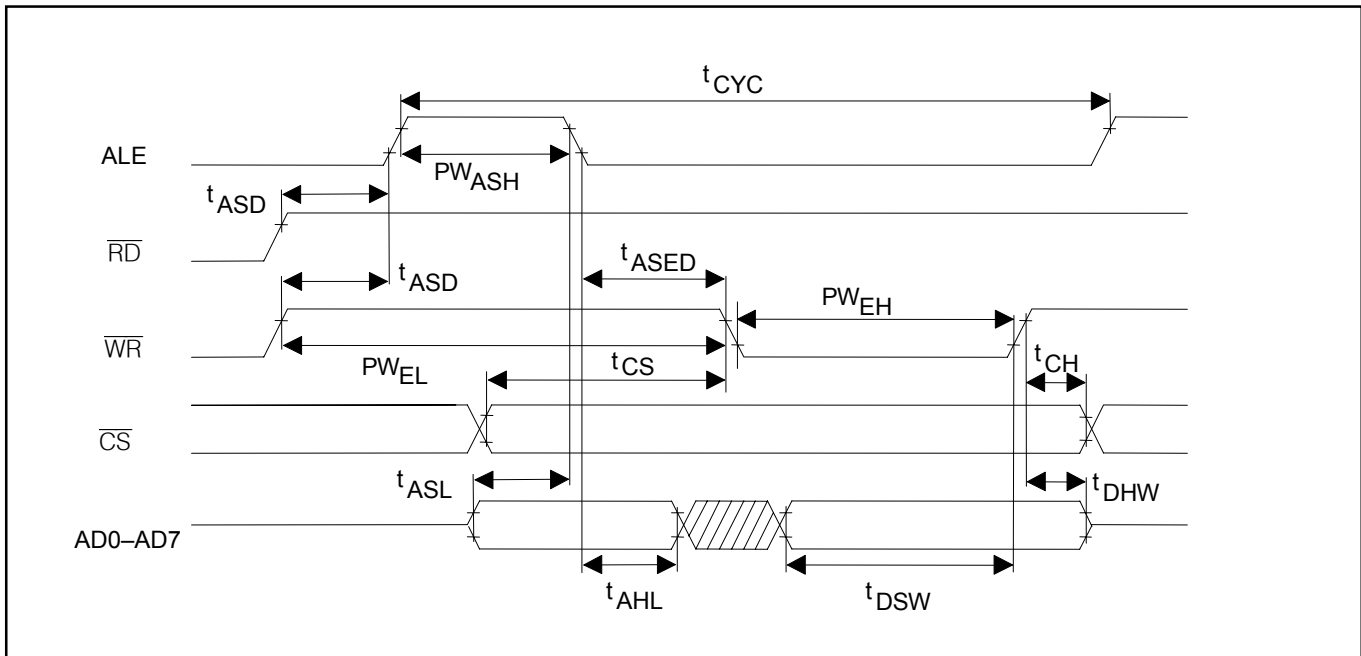
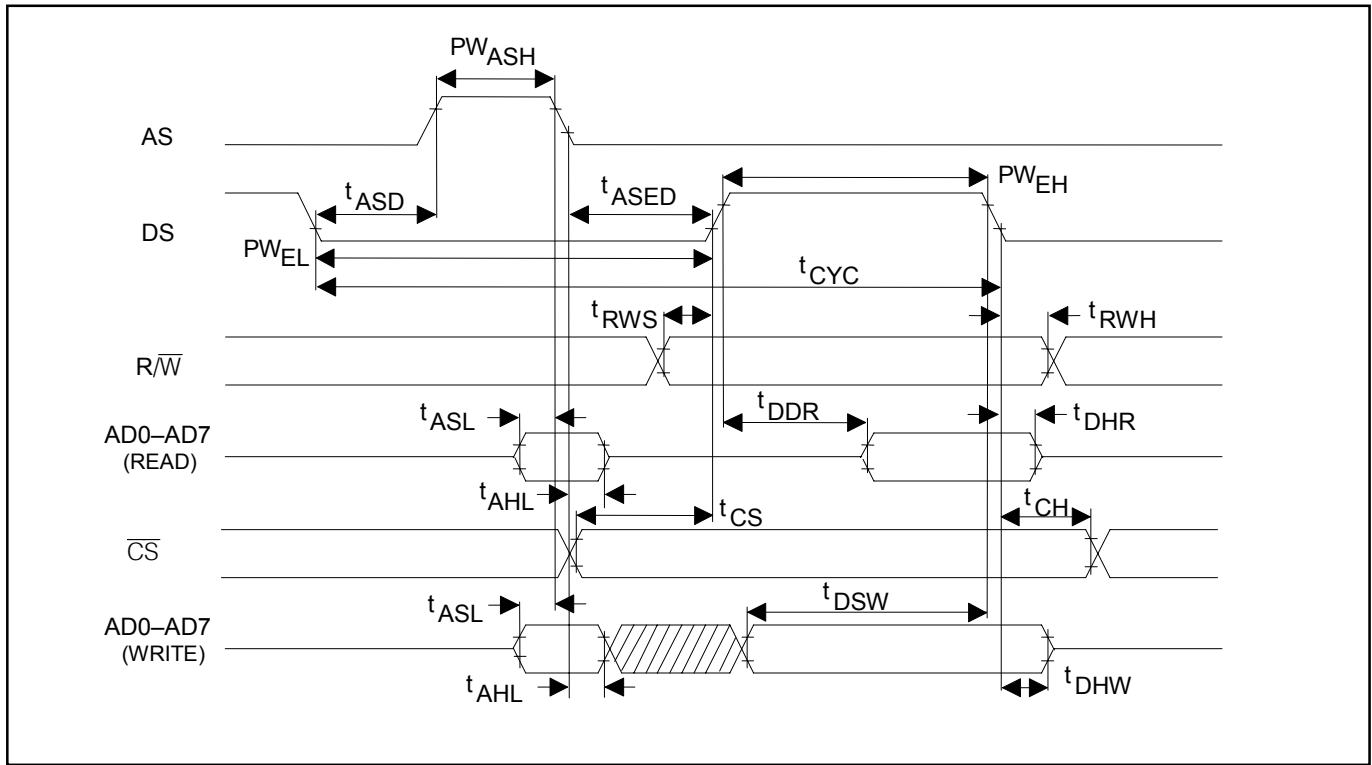


Figure 26-3. Motorola Bus AC Timing (PBTS = 1)



26.2 Nonmultiplexed Bus AC Characteristics

Table 26-B. AC Characteristics—Nonmultiplexed Parallel Port

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)

(Figure 26-4 through Figure 26-7)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|------------|-----|-----|-----|-------|
| Setup Time for A0 to A7, Valid to \overline{CS} Active | t1 | | 0 | | | ns |
| Setup Time for \overline{CS} Active to Either \overline{RD} , \overline{WR} , or \overline{DS} Active | t2 | | 0 | | | ns |
| Delay Time from Either \overline{RD} or \overline{DS} Active to Data Valid | t3 | | | | 140 | ns |
| Hold Time from Either \overline{RD} , \overline{WR} , or \overline{DS} Inactive to \overline{CS} Inactive | t4 | | 0 | | | ns |
| Hold Time from \overline{CS} Inactive to Data Bus Tri-State | t5 | | 5.0 | | 20 | ns |
| Wait Time from Either \overline{WR} or \overline{DS} Active to Latch Data | t6 | | 75 | | | ns |
| Data Setup Time to Either \overline{WR} or \overline{DS} Inactive | t7 | | 10 | | | ns |
| Data Hold Time from Either \overline{WR} or \overline{DS} Inactive | t8 | | 10 | | | ns |
| Address Hold from Either \overline{WR} or \overline{DS} Inactive | t9 | | 10 | | | ns |

Figure 26-4. Intel Bus Read Timing (PBTS = 0)

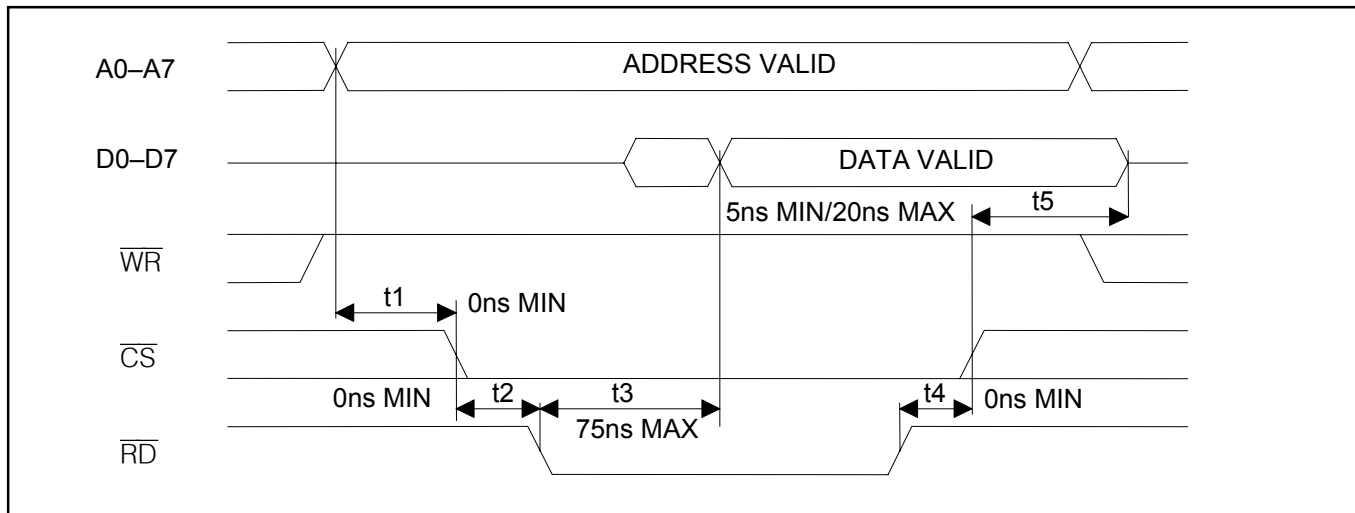


Figure 26-5. Intel Bus Write Timing (PBTS = 0)

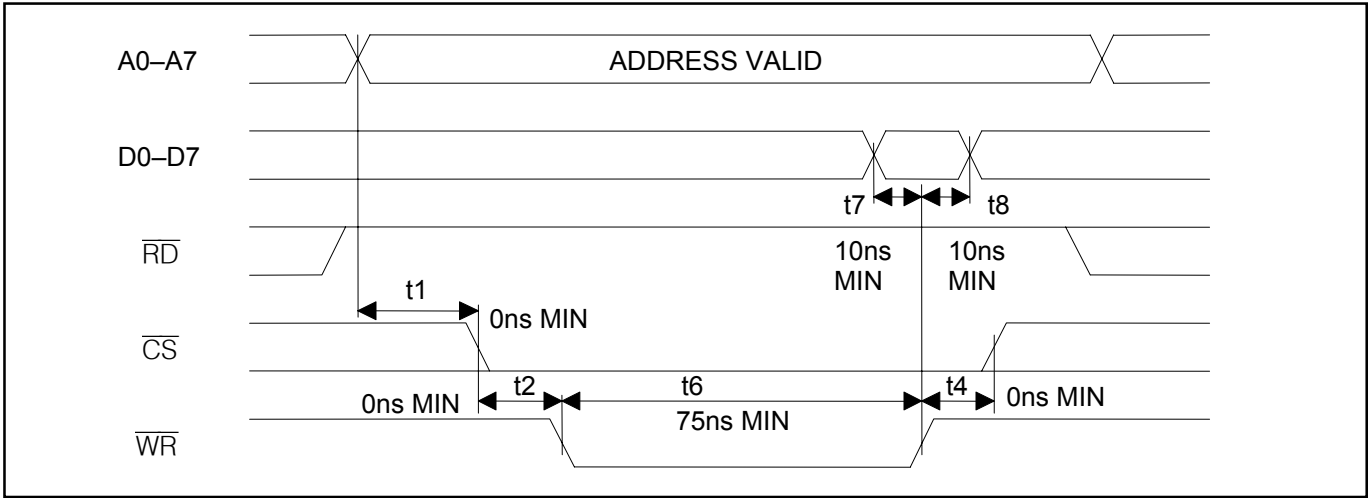


Figure 26-6. Motorola Bus Read Timing (PBTS = 1)

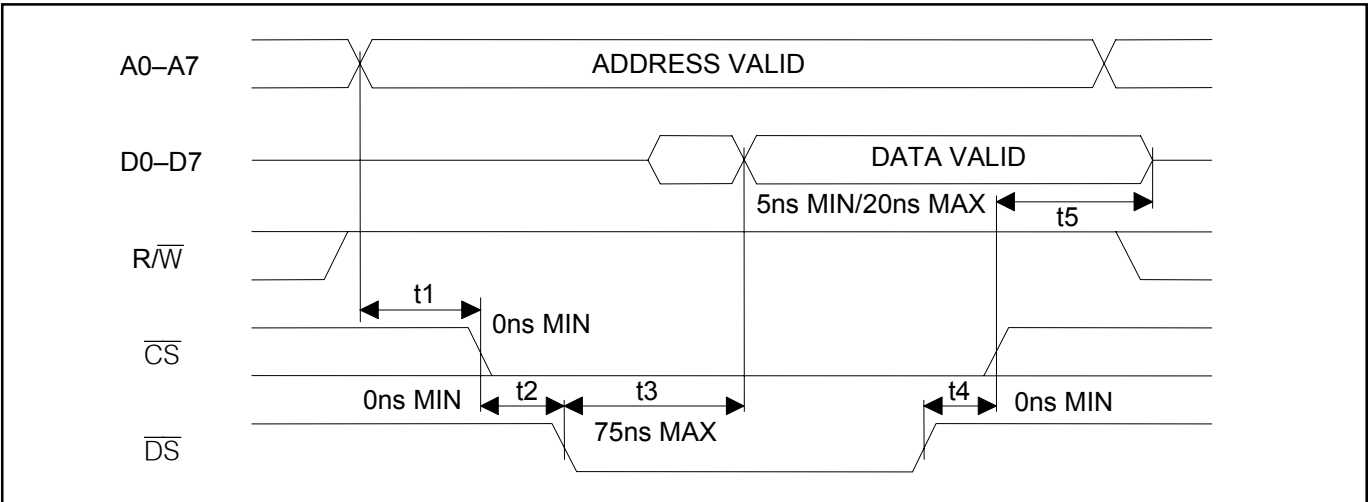
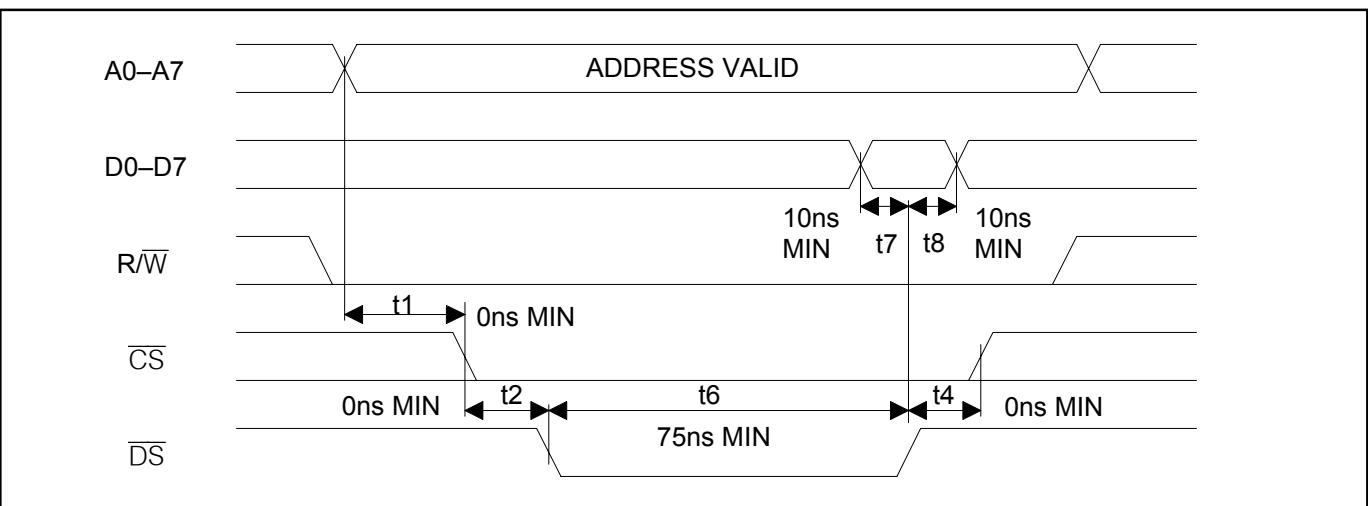


Figure 26-7. Motorola Bus Write Timing (PBTS = 1)



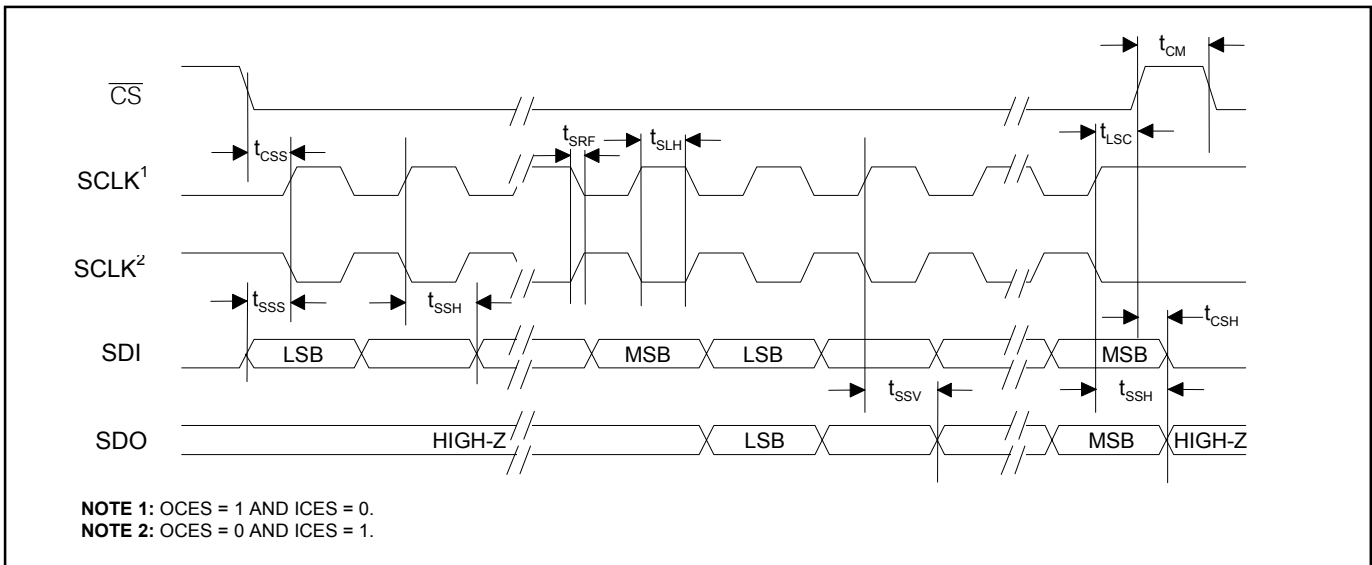
26.3 Serial Port

Table 26-C. AC Characteristics—Serial Port (BTS1 = 1, BTS0 = 0)

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)
 (Figure 26-8)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|------------|-----|-----|-----|-------|
| Setup Time \overline{CS} to SCLK | t_{CSS} | | 50 | | | ns |
| Setup Time SDI to SCLK | t_{SSS} | | 50 | | | ns |
| Hold Time SCLK to SDI | t_{SSH} | | 50 | | | ns |
| SCLK High/Low Time | t_{SLH} | | 200 | | | ns |
| SCLK Rise/Fall Time | t_{SRF} | | | | 50 | ns |
| SCLK to \overline{CS} Inactive | t_{LSC} | | 50 | | | ns |
| \overline{CS} Inactive Time | t_{CM} | | 250 | | | ns |
| SCLK to SDO Valid | t_{SSV} | | | | 50 | ns |
| SCLK to SDO Tri-State | t_{SSH} | | | 100 | | ns |
| \overline{CS} Inactive to SDO Tri-State | t_{CSH} | | | 100 | | ns |

Figure 26-8. Serial Bus Timing (BTS1 = 1, BTS0 = 0)



26.4 Receive AC Characteristics

Table 26-D. AC Characteristics—Receiver

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)

([Figure 26-9](#) and [Figure 26-10](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------|----------|------------|-----|--------------|-----|-------|
| SYSCLK Period | t_{SP} | (Note 1) | | 648 | | ns |
| | | (Note 2) | | 488 | | |
| | | (Note 3) | | 244 | | |
| | | (Note 4) | | 122 | | |
| | | (Note 5) | | 61 | | |
| SYSCLK Pulse Width | t_{SH} | | 20 | $0.5 t_{SP}$ | | ns |
| | t_{SL} | | 20 | $0.5 t_{SP}$ | | |
| RSYNC Setup to SYSCLK Falling | t_{SU} | | 20 | | | ns |
| RSYNC Hold from SYSCLK Falling | t_{HD} | | 20 | | | ns |
| RSYNC Pulse Width | t_{PW} | | 50 | | | ns |
| Delay RCLK to RSER Valid | t_{D1} | | | | 50 | ns |
| Delay RCLK to RSYNC, OUTA, OUTB | t_{D2} | | | | 50 | ns |
| Delay SYSCLK to RSER Valid | t_{D3} | | | | 22 | ns |
| Delay SYSCLK to RSYNC, OUTA, OUTB | t_{D4} | | | | 22 | ns |

Note 1: SYSCLK = 1.544MHz.

Note 2: SYSCLK = 2.048MHz.

Note 3: SYSCLK = 4.096MHz.

Note 4: SYSCLK = 8.192MHz.

Note 5: SYSCLK = 16.384MHz.

Figure 26-9. Receive AC Timing (Receive Elastic Store Disabled)

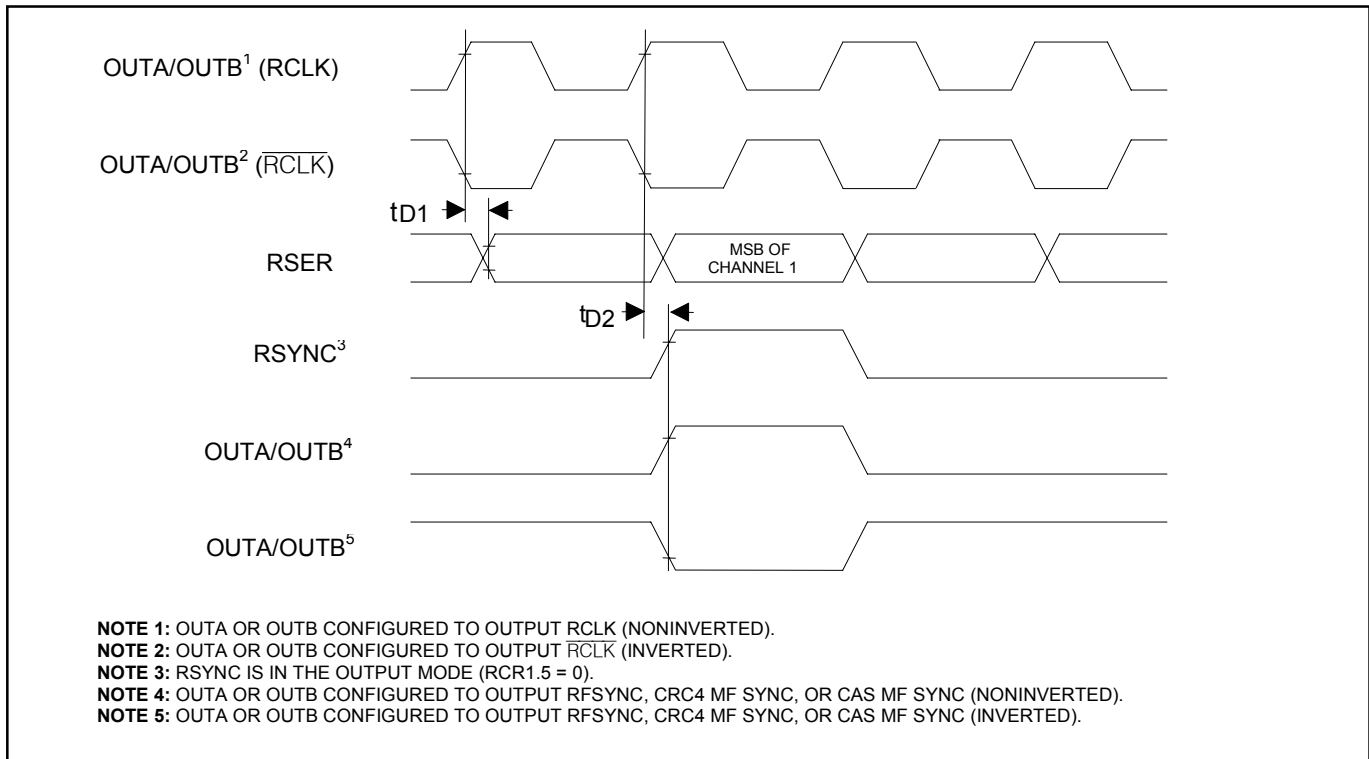
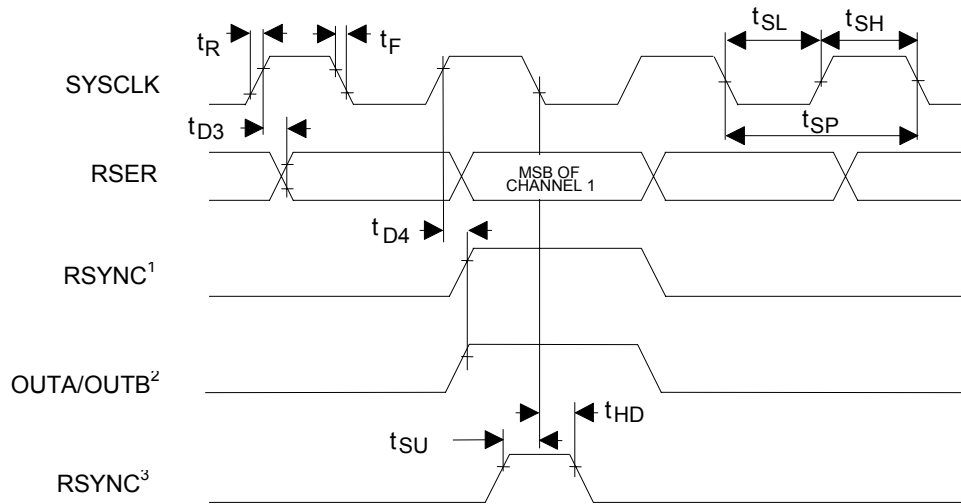


Figure 26-10. Receive AC Timing (Receive Elastic Store Enabled)



- NOTE 1:** RSYNC IS IN THE OUTPUT MODE (RCR.5 = 0).
- NOTE 2:** OUTA OR OUTB CONFIGURED AS CRCR MF SYNC OR CAS MF SYNC.
- NOTE 3:** RSYNC IS IN THE INPUT MODE (RCR.5 = 1).

26.5 Transmit AC Characteristics

Table 26-E. AC Characteristics—Transmit

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)

([Figure 26-11](#) and [Figure 26-12](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|------------|------------|-----|--------------|-----|-------|
| TCLK Period | t_{CP} | (Note 1) | | 648 | | ns |
| | | (Note 2) | | 488 | | |
| TCLK Pulse Width | t_{CH} | | 20 | $0.5 t_{CP}$ | | ns |
| | t_{CL} | | 20 | $0.5 t_{CP}$ | | |
| SYSCLK Period | t_{SP} | (Note 1) | | 648 | | ns |
| | | (Note 2) | | 488 | | |
| | | (Note 3) | | 244 | | |
| | | (Note 4) | | 122 | | |
| | | (Note 5) | | 61 | | |
| SYSCLK Pulse Width | t_{SH} | | 20 | $0.5 t_{SP}$ | | ns |
| | t_{SL} | | 20 | $0.5 t_{SP}$ | | |
| TSYNC Setup to TCLK | t_{SU} | | 20 | | | ns |
| TSYNC Pulse Width | t_{PW} | | 50 | | | ns |
| TSER Setup to TCLK or SYSCLK Falling | t_{SU} | | 20 | | | ns |
| TSER Hold from TCLK or SYSCLK Falling | t_{HD} | | 20 | | | ns |
| TCLK Rise and Fall Times | t_R, t_F | | | | 25 | ns |

Note 1: SYSCLK = 1.544MHz.

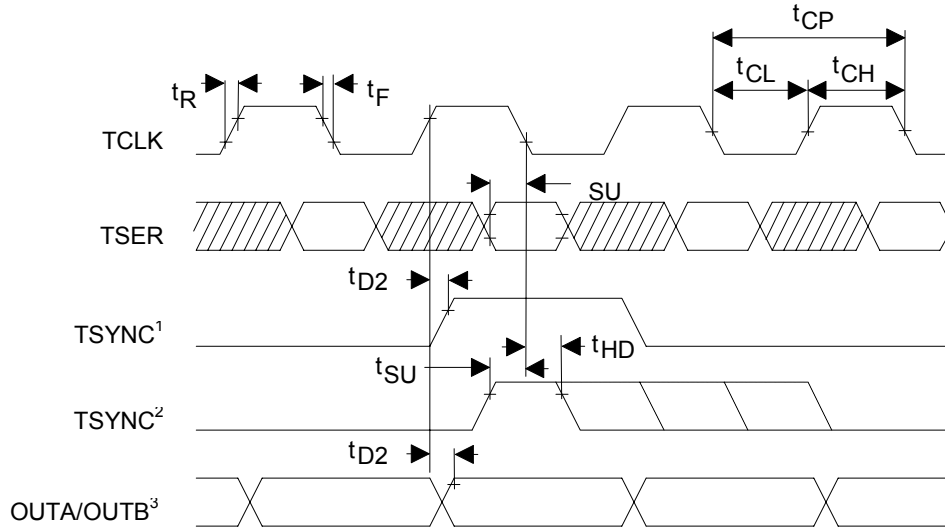
Note 2: SYSCLK = 2.048MHz.

Note 3: SYSCLK = 4.096MHz.

Note 4: SYSCLK = 8.192MHz.

Note 5: SYSCLK = 16.384MHz.

Figure 26-11. Transmit AC Timing (IBO Disabled)

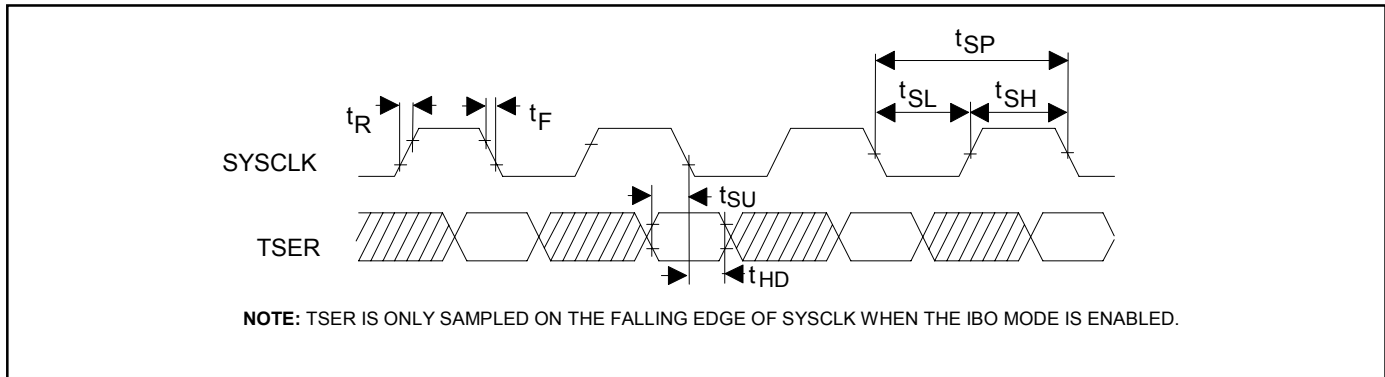


NOTE 1: TSYNC IS IN OUTPUT MODE (TCR.0 = 1).

NOTE 2: TSYNC IS IN INPUT MODE (TCR.0 = 0). TSYNC MAY BE HELD HIGH FOR MULTIPLE CLOCK CYCLES AS LONG AS IT TRANSITIONS LOW AT LEAST TWO CLOCK CYCLES BEFORE TRANSITIONING HIGH AGAIN.

NOTE 3: APPLIES TO OUTA AND OUTB WHEN CONFIGURED FOR TPOS AND TNEG OUTPUTS.

Figure 26-12. Transmit AC Timing (IBO Enabled)



26.6 Special Modes AC Characteristics

Table 26-F. AC Characteristics—Special Modes

($V_{DD} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$ for DS21Q59L; $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$ for DS21Q59LN.)

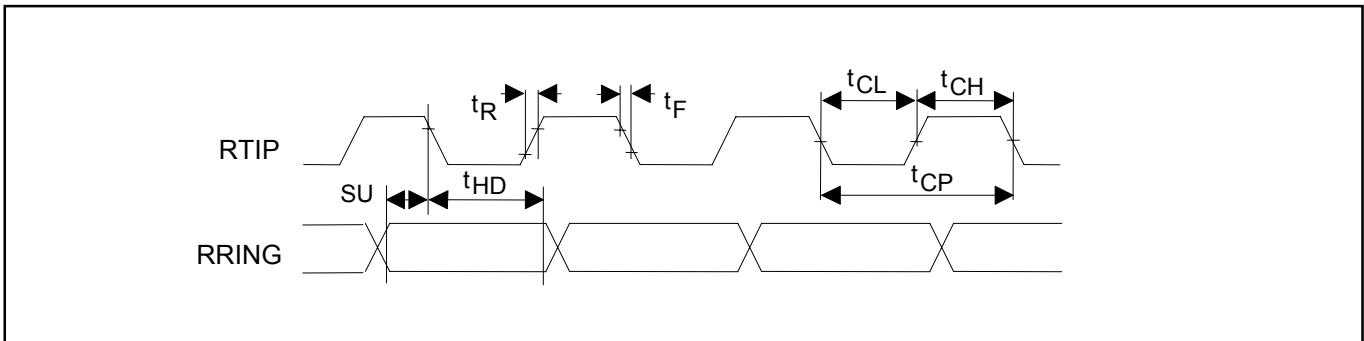
([Figure 26-13](#))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|------------|------------|-----|-----|-----|-------|
| RTIP Period | t_{CP} | | | 488 | | ns |
| RTIP Pulse Width | t_{CH} | | 75 | | | ns |
| | t_{CL} | | 75 | | | |
| RTIP Setup to RRING Falling | t_{SU} | | 20 | | | ns |
| TSER Hold from TCLK Falling | t_{HD} | | 20 | | | ns |
| RTIP, RRING Rise and Fall Times | t_R, t_F | | | | 25 | ns |

Special Mode: OUTBC.7 = 1.

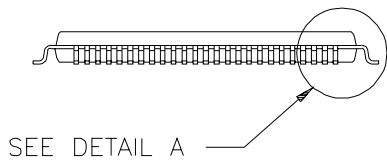
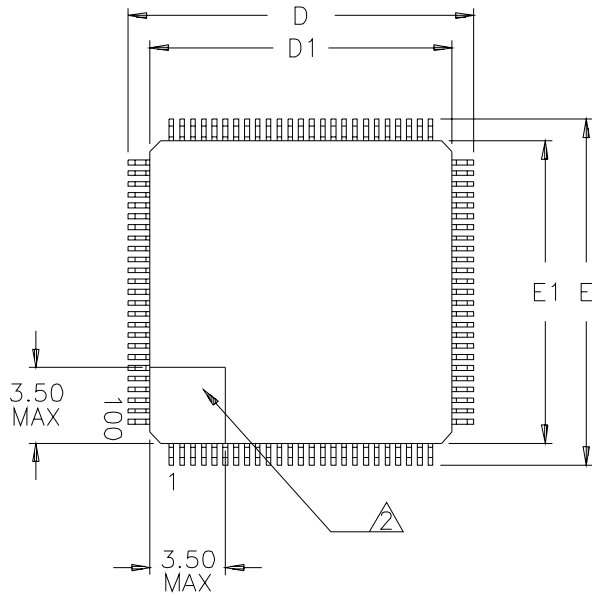
Note: RTIP and RRING become NRZ data and clock inputs.

Figure 26-13. NRZ Input AC Timing



27. PACKAGE INFORMATION

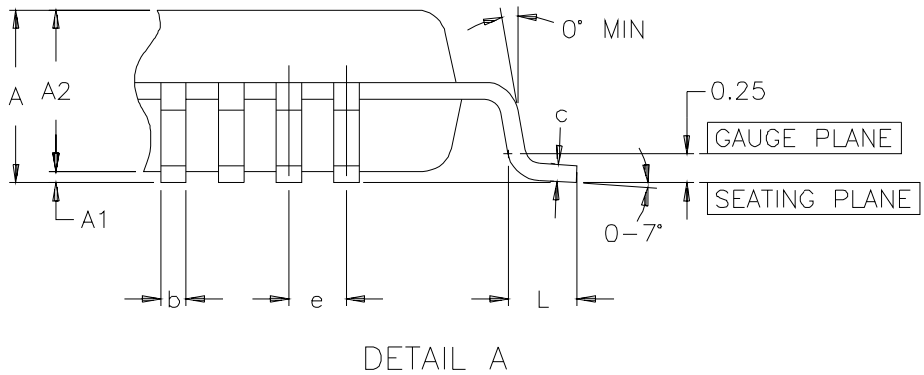
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/DallasPackInfo.)



NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
3. ALLOWABLE DAMBAR PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION; PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OR FOOT OF LEAD.
4. ALL DIMENSIONS ARE IN MILLIMETERS.

| DIM | MIN | MAX |
|-----|-------|-------|
| A | — | 1.60 |
| A1 | 0.05 | — |
| A2 | 1.35 | 1.45 |
| b | 0.17 | 0.27 |
| c | 0.09 | 0.20 |
| D | 15.80 | 16.20 |
| D1 | 14.00 | BSC |
| E | 15.80 | 16.20 |
| E1 | 14.00 | BSC |
| e | 0.50 | BSC |
| L | 0.45 | 0.75 |



28. REVISION HISTORY

| DATE | DESCRIPTION |
|--------|---|
| 042403 | New product release. |
| 090104 | 1) Add 16MHz IBO timing diagram and AC characteristics 2) Correct typos in Figure 26-10. Reference to RSYNC as an input, not an output as shown in Note 3. 3) Added clarification to Section 23 regarding the TSYNCx pin when the part is configured for IBO mode. 4) Modified Table 26-D for clarification and corrected values. 5) Modified Table 26-E for clarification and corrected values. 6) Added tHD parameter to Figure 26-12. 7) Added Notes to Figures 24-3, 24-4, 24-6, 24-7, 26-11 regarding the duration of the Sync pin when configured as an input. 8) Corrected typo on Figure 24-4 Note 3, incorrect bit value for RSYNC configured as an input. (should be RCR.5 = 1). |

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